DDR3 4Gbit (256Mx16)

MB24G16DBR-XXXXC

MB24G16DBR-1600C Datasheet

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1. Revision History

Revison	History	Date
1.0	Preliminary release	2019/7/17

2. Features

- Double-data-rate architecture: two data transfers Per clock cycle
- The high-speed data transfer is realized by the 8 Bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; centeraligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality On-Die Termination (ODT) for better signal quality
    - Synchronous ODT
    - Dynamic ODT
    - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for Power-up sequence and reset function
- SRT range: Normal/extended
- Programmable Output driver impedance control

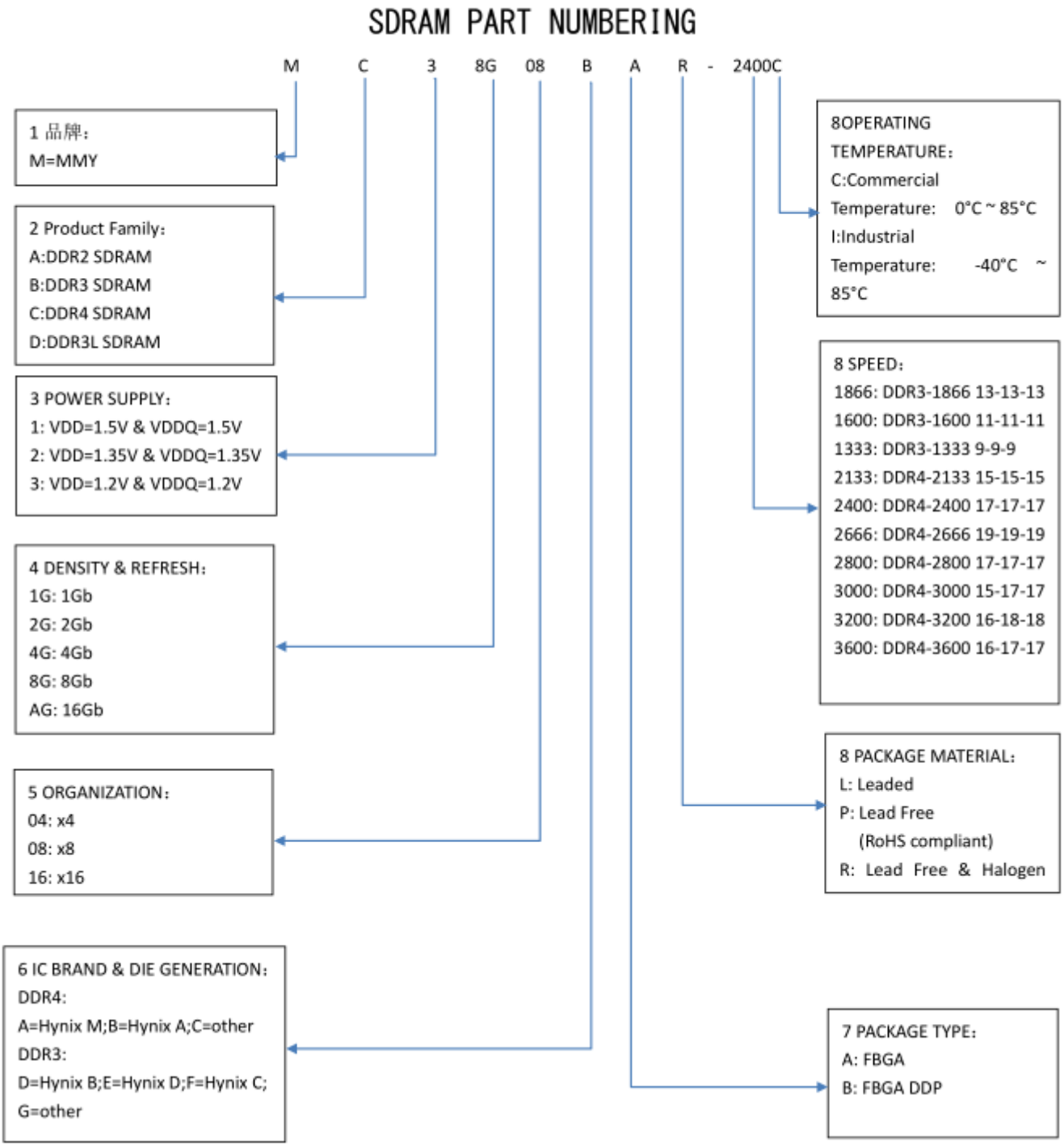
3. Contents

4. Ordering Information

Table 1: product list

Mentor Series			
Part Number	Density	Package Size / Thickness	Package Type / Ballout
MB24G16DBR-1600C	4 Gbit	7.5x13x1.1 mm	96-ball FBGA

5. Part Number Decoder

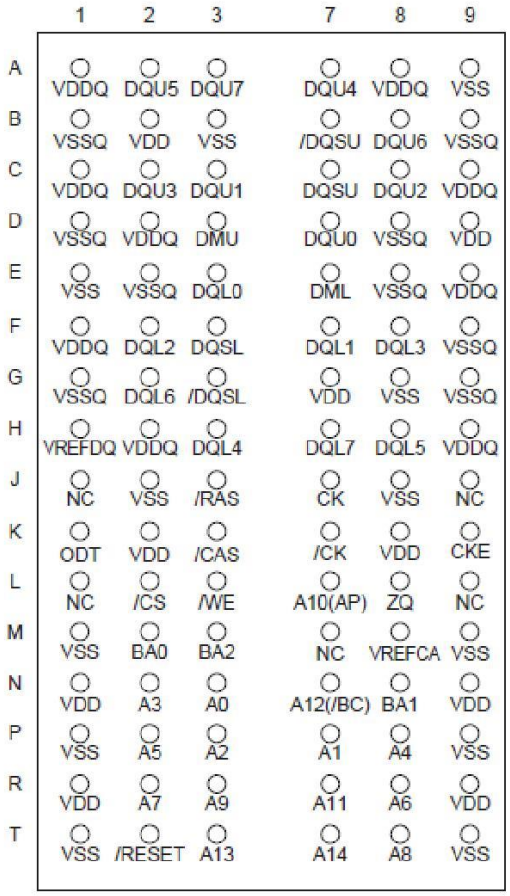


6. Specifications

- Density: 4G bits
- Organization: 32M words 16 bits 8 banks
- Package: 96-ball FBGA
  Lead-free (RoHS compliant) and Halogen-free
- Power supply: VDD, VDDQ =1.35V +/-0.075V
- Data rate: 1333Mbps/1600Mbps/1866Mbps (max.)
- 2KB page size: Row address: A0 to A14
  Column address: A0 to A9
- Eight internal banks for concurrent operation
- Interface: SSTL_15
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT): Sequential (8, 4 with BC)
  Interleave (8, 4 with BC)
- CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11
- CAS Write Latency (CWL): 5, 6, 7, 8
- Precharge: auto precharge option for each Burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles: Average refresh period
  7.8us at 0℃ ≤TC ≤+85℃
  3.9us at+85℃ TC ≤+95℃

Operating case temperature : range TC = 0℃ to +95℃

7. Pin Configurations



96-ball FBGA (Top view)

Pin name	Function	Pin name	Function
A0 to A14*2	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET*2	Active low asynchronous reset
BA0 to BA2*2	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	Data input/output	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS*2	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE*2	Command input	VREFDQ	Reference voltage for DQ
CKE*2	Clock enable	VREFCA	Reference voltage
CK, /CK	Differential clock input	ZQ	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC*1	No connection
ODT*2	ODT control		

Notes: 1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

8. Package Drawing

96-ball FBGA -- Solder ball: Lead free (Sn-Ag-Cu)