



TR4P153BT/BF General Purpose MCU

1. General Descriptions

The TR4P153BT/BF series are high-performance 4-bit RISC micro-controller embedded with 2KX12 bits OTP, 256X4 bits SRAM, 8 bit PWM, 11 Input/Output ports and one input port. It's flexible and cost-effective solution for general purpose MCU applications.

2. Features

- Operating voltage: (1) 2.0V to 5.5V for Temp. = 25 (2) 2.2V to 5.5V for Temp. = -40 ~+85
- These MCU can operate in high speed. Oscillator type can be selected by option setting. High speed and low speed operating mode is selectable by software. Below is the chip performance in different modes.
 - (a) Internal high speed HRCOSC: 8 MIPS / 4 MIPS / 2 MIPS / 1 MIPS or low speed LRCOSC 114.69KIPS(thousand instructions per second) / 57.34 KIPS / 28.67 KIPS / 14.33 KIPS.
 - (b) External EXTOSC: 8 MIPS (16 MHz X'tal) ~ 0.5 MIPS (1 MHz X'tal).
- Memory Size
 - Program ROM size : 2KX12 bits (OTP type)
 - SRAM size: total 256x4 bits SRAM
- Wake up function for power-down mode
 - HALT mode wake up source: RTC timer overflow, PA0~3, PB0~3 and PD0~3 edge trigger
- 11 input /output ports: PA0~PA2, PB0~PB3, PD0~PD3. Each I/O can be bit programmable as input or output port. These 11 I/Os also provided level-change-wakeup function. Pull up and pull down resistor setting is available by software.
- 1 input port PA3, PA3 is shared with RSTB (reset) pin by option. It also provides level-change-wakeup function. Pull up and pull down resistor can be configured by software too.
- Port A, Port B and Port D are provided with high sink current 24mA @VDD=5V, Vol=0.5V(except PA3)
- Port A, Port B and Port D are provided with high drive current 23mA @VDD=5V, Voh=4.5V(except PA3)
- PA1 built-in 38KHz modulator by option.
- One Op-Amp is provided, three pins shared with PD0, PD1, PB2 (by option).
- One comparator is provided, two input pins shared with PD2, PD3 (by option).
- Three timers
 - Timer 1: 8 bits timer/counter/PWM, its clock source can be from chip-internal or external.
 - Timer 2: 8 bits timer
 - RTC : time period 0.125 /0.25/0.5/1 Sec or 15.625/31.25/62.5/125 ms, RTC Clock source comes from internal LRCOSC.
- Four reset condition
 - Low voltage reset (LVR 1.8V)
 - Power on reset
 - External RSTB pin shared with PA3 pin by option.
 - Watch dog timer overflow reset (0.125 sec ~ 1 sec by option)
- Three internal interrupt sources: TIMER1, TIMER2 or RTC interrupt.
- WDT(Watch dog timer)
 - WDT can be enabled/disabled in HALT mode by option
 - WDT clock source comes from internal LRCOSC.
- Provides 8 Bits PWM, PWM signal output is shared with PA2 pin by option.
- Built-in external X'tal oscillator (EXTOSC, use 1MHz~16MHz external ceramic resonator or crystal oscillator). These two crystal pins are shared with PB1 and PB0 by option.
- Built-in high frequency internal 32MHz RC oscillator (HRCOSC, frequency deviation within ±2%, temperature range at -40 ~+85 , Vdd = 2.0V to 5.5V)
- Built-in low frequency internal RC OSC (LRCOSC) 459KHz (frequency deviation within ±12%)

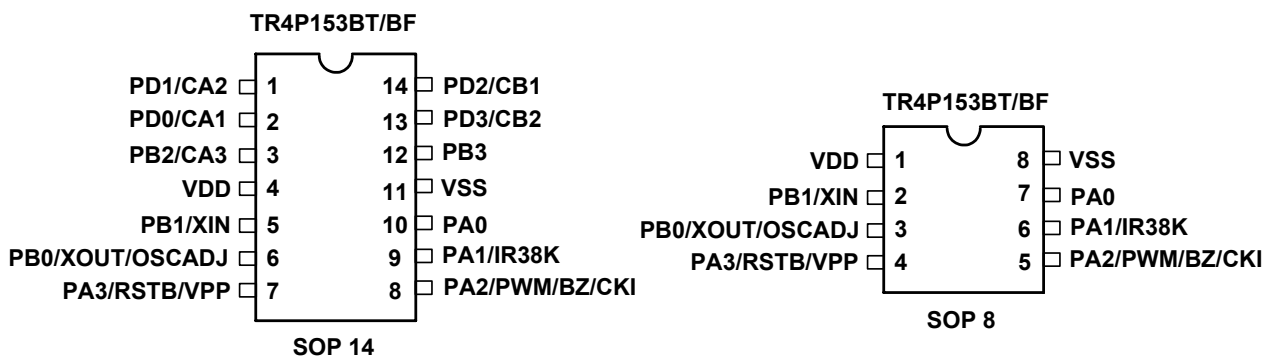


Selection table

| Feature \ P/N | TR4P153BT | TR4P153BF |
|-----------------------------------|-----------------------------------|-------------------------|
| Real OTP ROM size | 1.6K words (1536 x 12 + 48X12) | 2K words (1984 X 12) |
| User Information block (Note 1) | Yes | No |
| reusable COB by UV erasing | No | Yes |
| SRAM | 256 x 4 bits | |
| I/O Pins | 11 I/O and 1 Input PIN | |

Note 1 : Support user Information block (48X12 bits) for serial number, lot number or user optional codes ...etc. It's located at address 640h ~ 66Fh.

Package (8/14 SOP)

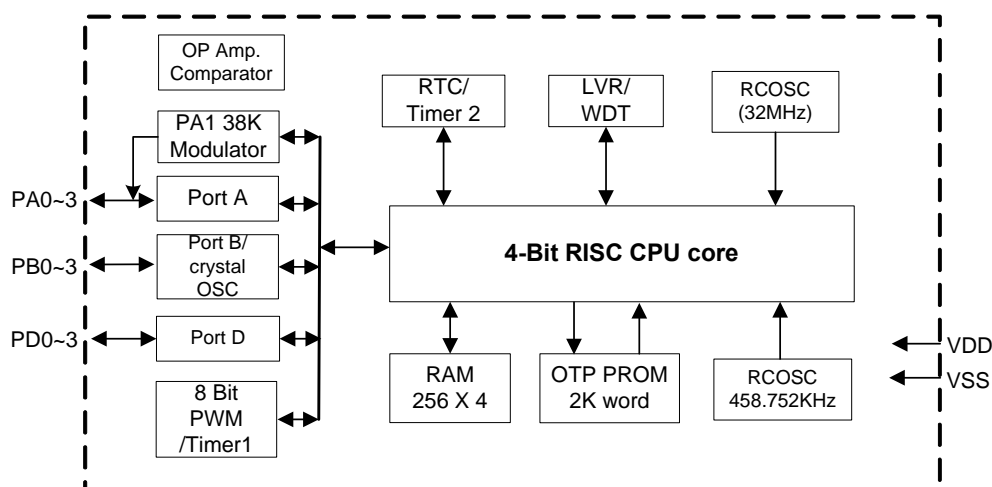




3. Pads Information

| PAD Name | Type | State After Reset | Description |
|--------------------------|------|-------------------|--|
| Power Input | | | |
| VDD | I | High | Power input pin |
| VSS | I | Low | Ground input pin |
| General I/O ports | | | |
| PA0~PA2 | I/O | XXX | PA0~PA2 are programmable I/O ports, with pull up and down resistor 100K ohm. Level-change-wakeup function is provided. PA1 is shared with IR38K function by option. PA2 is shared with PWM/CKI/BZ functions by option. |
| PA3 (RSTB/VPP) | I | X | PA3 is an input pin only, with pull up resistor 60K ohm, or pull down resistor 100K ohm. Level-change-wakeup function is provided. PA3 is shared with RSTB pin by option. |
| PB0~PB3 | I/O | XXXX | PB0~PB3 are programmable I/O ports, with pull up and down resistor 100K ohm. Level-change-wakeup function is provided. PB0 is shared with XOUT/OSCADJ by option. OSCADJ pin is used for frequency adjust of HRCOSC. PB1 is shared with XIN pin by option. XIN and XOUT is connected to external X'tal. PB2 is shared with the output CA3 of Op Amp by option. |
| PD0~PD3 | I/O | XXXX | Port D is a programmable I/O port, with pull up and down resistor 100K ohm. Level-change-wakeup function is provided. PD0 and PD1 are shared with two inputs (CA1, CA2) of Op AMP by option. PD2 and PD3 are shared with two inputs (CB1, CB2) of a comparator by option. |

Block Diagram





4. ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|-----------------------|------------------|-----------------|------|
| DC Supply Voltage | V+ | < 7.0 | V |
| Input Voltage Range | V _{IN} | -0.5 to VDD+0.5 | V |
| Operating Temperature | T _A | -40 to +85 | °C |
| Storage Temperature | T _{STO} | -50 to +150 | °C |

4.2 DC/AC Characteristics

DC CHARACTERISTICS (T_A = 25 , VDD = 3V, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMIT | | | UNIT |
|--------------------------------------|---------------------|---|---------------------|----------------------------|---------------------|-------|
| | | | Min | Typ | Max | |
| Operating voltage | V _{VDD1} | Temp. = 25 | 2.0 | - | 5.5 | V |
| | V _{VDD2} | Temp.= -40 ~+85 | 2.2 | | 5.5 | V |
| Operating Current | I _{OP1} | VDD=3V , MCU run 8 MIPS | | 2.6 | | mA |
| | I _{OP2} | VDD=5V , MCU run 8 MIPS | | 3.0 | | mA |
| | I _{OP3} | VDD=3V , MCU run 1 MIPS | | 1.6 | | mA |
| | I _{OP4} | VDD=5V , MCU run 1 MIPS | | 2.0 | | mA |
| | I _{OP5} | VDD=3V , MCU run 14 KIPS | | 50 | | uA |
| | I _{OP6} | VDD=3V , MCU run 114.7 KIPS | | 200 | | uA |
| Standby Current | I _{STBY1} | MCU stop in HALT mode WDT & RTC off | | 2.5 (VDD=3V) 3 (VDD=5V) | | uA |
| | I _{STBY2_} | 1.VDD=5V 2.MCU stop in HALT mode, WDT on or RTC on | | 8 | | uA |
| Input High Level | V _{IH} | All I/O port | 0.8*V _{DD} | | | V |
| Input Low Level | V _{IL} | All I/O port | | | 0.2*V _{DD} | V |
| Output Drive Current | I _{OH1} | VDD=3V , V _{OH} =2.5V, All I/O port | -8 | -15 | | mA |
| | I _{OH2} | VDD=5V , V _{OH} =4.5V, All I/O port | -12 | -23 | | mA |
| Output Sink Current | I _{OL1} | VDD=3V , V _{OL} =0.5V, All I/O port | 8 | 15 | | mA |
| | I _{OL2} | VDD=5V , V _{OL} =0.5V, All I/O port | 12 | 24 | | mA |
| PA,PB,PD pull down Res. | R _{down1} | Pull down 180K ohm, VDD=3V | 140 | 180 | 220 | K ohm |
| | R _{down2} | Pull down 100K ohm, VDD=5V | 60 | 90 | 120 | K ohm |
| PA,PB,PD pull up Res. (except PA3) | R _{up1} | Pull up 180K ohm, VDD=3V | 140 | 180 | 220 | K ohm |
| | R _{up2} | Pull up 100K ohm, VDD=5V | 60 | 90 | 120 | K ohm |
| PA3 pull up Res. | R _{up3} | Pull up 60K ohm ,VDD=2V~5V | 40 | 60 | 80 | K ohm |
| LVR | V _{LVR1} | Temp. = 25 | 1.6 | 1.8 | 2.0 | V |
| | V _{LVR2} | Temp.= -40 ~+85 | 1.4 | 1.8 | 2.2 | V |



AC characteristics (TA = 25 , VDD = 3V, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMIT | | | UNIT |
|---|----------------------|---|-------|--|-------|------|
| | | | Min | Typ | Max | |
| Internal HRCOSC Frequency | F _{HRCOSC} | VDD = 2.0V~5.5V Temp = -40 ~+85 | 31.36 | 32 ±2% | 32.64 | MHz |
| Internal LRCOSC Frequency | F _{LRCOSC1} | VDD = 2.0V~5.5V Temp. = 25 | | 458.752 ±12% | | KHz |
| | F _{LRCOSC2} | VDD = 2.0V~5.5V Temp = -40 ~+85 | | 458.752 ±20% | | KHz |
| External X'tal EXTOSC | F _{XTOSC} | VDD = 2.0V~5.5V | | 1~16 | | MHz |
| MCU operating frequency (clock source from F _{HRCOSC} or F _{XTOSC}) | F _{MCK1} | 1.in NORMAL mode 2.Clock source : F _{HRCOSC} 3.VDD = 2.0V~5.5V 4.Temp. -40 ~+85 | | 8 ±2%, 4 ±2% 2 ±2%, 1 ±2% (F _{HRCOSC} /4, F _{HRCOSC} /8, F _{HRCOSC} /16, F _{HRCOSC} /32) | | MIPS |
| | F _{MCK2} | 1.in NORMAL mode 2.Clock source : F _{XTOSC} 3.VDD = 2.0V~5.5V 4 Temp. -40 ~+85 5.If F _{XTOSC} = 16Mhz | | 8 , 4 , 2 , 1 (F _{XTOSC} /2, F _{XTOSC} /4, F _{XTOSC} /8, F _{XTOSC} /16) | | MIPS |
| MCU operating frequency (clock source F _{LRCOSC}) | F _{MCK3} | 1.in GREEN mode 2.VDD = 2.0V~5.5V 3.Temp. = 25 | | 114.69±12%, 57.34±12% 28.67±12%, 14.33±12% | | KIPS |
| PA1 38KHz output (clock source F _{HRCOSC} Or F _{XTOSC}) | F _{38K1} | 1.in NORMAL mode 2.PA1 IR38K option enabled 3.Register F38K=1 4.Temp. = 25 | | 38.09 ±2% (F _{HRCOSC} /840) | | KHz |
| | | | | 38.09 (F _{XTOSC} =16Mhz)/420 | | |
| PA1 38KHz output (clock source F _{LRCOSC}) | F _{38K2} | 1.in GREEN mode 2.PA1 IR38K option enabled 3.Register F38K=1 4.Temp. = 25 | | 38.23 ±12% (F _{LRCOSC} /12) | | KHz |
| RTC period | T _{RTC1} | VDD = 2.0V~5.5V Temp. = 25 clock source F _{LRCOSC} SPUP option enabled | | 0.125±12%, 0.25±12% 0.5±12%, 1.0±12% | | Sec |
| | T _{RTC2} | VDD = 2.0V~5.5V Temp. = 25 clock source F _{LRCOSC} SPUP option disabled | | 15.625±12%, 31.25±12% 62.5±12%, 125±12% | | ms |
| WDT period | T _{WDT} | VDD = 2.0V~5.5V Temp. = 25 clock source F _{LRCOSC} | | 0.125±12%, 0.25±12% 0.5±12% , 1.0±12% | | Sec |
| Stable clock delay after power on or system reset | CKstable1 | System oscillator --HRCOSC (Note 1) | | 160us + 1024 x (1/ F _{MCK1}) (Note 5) | | us |
| | CKstable2 | System oscillator --EXTOSC (Note 2) | | 160us + 1024 x (1/ F _{MCK2}) (Note 5) | | us |
| Stable clock delay after wake up | CKstable3 | System oscillator --HRCOSC (Note 3) | | 64 x (1/ F _{MCK1}) (Note 5) | | us |
| | CKstable4 | System oscillator --EXTOSC (Note 4) | | 1024 x (1/ F _{MCK2}) (Note 5) | | us |



Note1: The stable clock delay (CKstable1) is a delay between HRCOSC-started and 1st instruction-execution.

This delay will ensure stable system clock after power on or reset.

Note2: The stable clock delay (CKstable2) is a delay between clock output of EXTOSC and 1st instruction. This delay will ensure stable system clock after power on or reset.

Note3: The stable clock delay (CKstable3) is a delay between HRCOSC-started and 1st instruction-execution of wakeup. This delay will ensure stable system clock after wake up.

Note4: The stable clock delay (CKstable4) is a delay between EXTOSC-started and 1st instruction-execution of wakeup. This delay will ensure stable system clock after wake up.

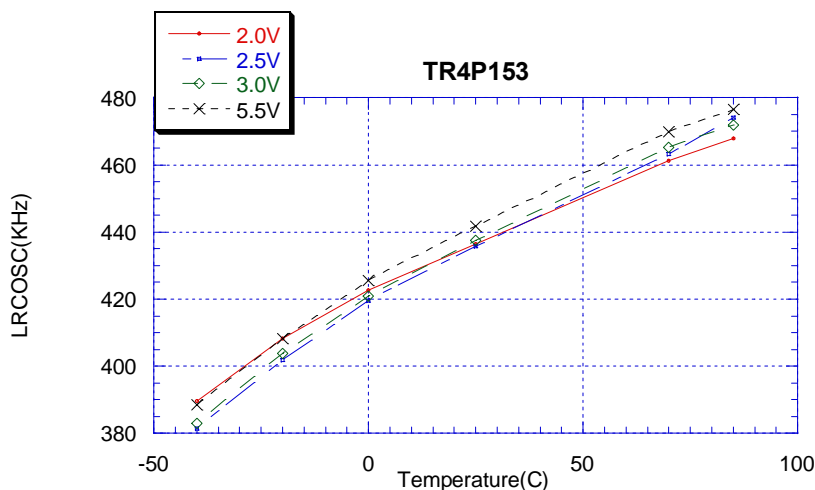
Note5: F_{MCK1} and F_{MCK2} are MCU operating clock.

AC Characteristics of OP ($T_A = 25$, $V_{DD} = 2V \sim 5.5V$, unless otherwise noted)

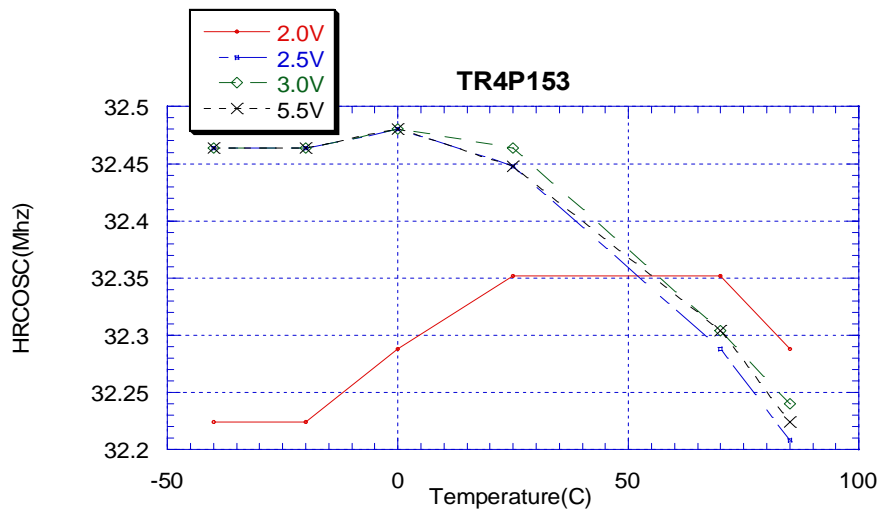
| PARAMETER | SYMBOL | TEST CONDITIONS | LIMIT | | | UNIT |
|-----------------------|------------|-------------------------|-------|-----|---------|---------|
| | | | Min | Typ | Max | |
| Quiescent current | I_{QUI} | $V_{DD} = 2V \sim 5.5V$ | 30 | 50 | 70 | μA |
| Input voltage range | V_{IN} | | 0 | | VDD | V |
| Output voltage range | V_{OUT} | | 0.1 | | VDD-0.1 | V |
| Offset voltage | V_{OS} | | 10 | | 100 | mV |
| Output sink current | I_{SINK} | | 15 | | 30 | μA |
| Output source current | I_{SOU} | | 150 | | 300 | μA |
| Output resistor load | R_L | | 100K | | | Ohm |

AC Characteristics of Comparator ($T_A = 25$, $V_{DD} = 2V \sim 5.5V$, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMIT | | | UNIT |
|---------------------|-----------|-------------------------|-------|-----|-----|---------|
| | | | Min | Typ | Max | |
| Quiescent current | I_{QUI} | $V_{DD} = 2V \sim 5.5V$ | 1 | | 2 | μA |
| Input voltage range | V_{IN} | | 0 | | VDD | V |
| Offset voltage | V_{OS} | | 10 | | 100 | mV |



The LRCOSC frequency VS. temperature, $V_{DD} = 2.0V \sim 5.5V$



The HRCOSC frequency VS. temperature, VDD=2.0V~5.5V

5. FUNCTIONAL DESCRIPTION

This MCU inside TR4P153BT/BF is a high performance processor. The operation speed can be range from 0.5 MIPS to 8 MIPS depending on different applications.

5.1 Program ROM (OTP ROM)

TR4P153B series support two kind of OTP ROM arrangement. They are TR4P153BT and TR4P153BF. The OTP ROM memory plan is shown below:

| Address | TR4P153BT (1.6 K OTP ROM) | TR4P153BF (2 K OTP ROM) |
|-------------|--|--------------------------------|
| 000h ~ 0FFh | User area 1.5K (1536 X12) | User area 1.5K (1536 X12) |
| 100h ~ 1FFh | | |
| 200h ~ 2FFh | | |
| | | |
| 500h ~ 5FFh | Reserved area | Reserved area |
| 600h ~ 63Fh | Reserved area | Reserved area |
| 640h ~ 66Fh | User Information block (48X12). For data store only, can't be used to store program. | User area 0.5K (448X12) |
| 670h ~ 7FFh | Reserved area | |

- Note: 1. For TR4P153BT and TR4P153BF, the content of OTP ROM address \$640h~\$66Fh can be read by program. Address \$600h~\$63Fh and \$670h~\$7FFh can't be read by program.
2. To read registers DMDL, DMDM and DMDH, only LD A,(n) instruction can be used. Other instructions are not allowed. (n = DMDL, DMDM or DMDH)
3. If DMA2~DMA0 pointed address is located at invalid address 600h~61Fh or 700h~7FFh, DMA2.2, DMA2.1, DMA2.0 will be regarded as 0 by hardware automatically, DMA0 and DMA1 will not be affected.



TR4P153BT supports 1.6 K words OTP ROM which is located on \$000h ~ \$5FFh and \$640h ~ \$66Fh. The first area \$000h ~ \$5FFh stores user program area. The second area \$640h ~ \$66Fh that named user information block stores serial number, lot number or user optional codes...etc. The reserved area are \$600h ~ \$63Fh and \$670h ~ \$7FFh, they can't be read by software.

TR4P153BF supports 2 K words OTP ROM which is located on \$000h ~ \$5FFh and \$640h ~ \$7FFh. These two areas store user program. Although \$640h~\$7FFh is user area, but data in \$670h~\$7FFh can't be read by software. The reserved area, \$600h ~ \$63Fh, can't be read by program also.

To read OTP ROM data, use DMA2~DMA0 registers as address pointer. The address range is located in \$000H ~ \$5FFH and \$640H~\$66FH. After these registers (DMA0~2) are specified by software, the 12bits data of ROM can be moved to A register by three instructions, they are "LD A, (DMDL)", "LD A, (DMDM)" and "LD A, (DMDH)". The three instructions mentioned above are two cycle instruction, all others instructions are single cycle instruction.

| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|-------------|------|-----|-------|--------|--------|--------|--------|---|
| DMA0 | 18H | R/W | xxxx | DMA0.3 | DMA0.2 | DMA0.1 | DMA0.0 | DMA0~DMA2(exclude DMA2.3) build a 11 bit addressing space for read ROM data. DMA0 is the lowest nibble address, DMA2 is the highest nibble address. DMA2.3: It's a user usable register only, it's useless for address setting. |
| DMA1 | 19H | R/W | xxxx | DMA1.3 | DMA1.2 | DMA1.1 | DMA1.0 | |
| DMA2 | 1AH | R/W | xxxx | DMA2.3 | DMA2.2 | DMA2.1 | DMA2.0 | |
| DMDL | 1CH | R | xxxx | DMDL.3 | DMDL.2 | DMDL.1 | DMDL.0 | DMDL is used to read low nibble data from ROM that addressed by DMA0 ~ DMA2. |
| DMDM | 1DH | R/W | xxxx | DMDM.3 | DMDM.2 | DMDM.1 | DMDM.0 | (1) DMDM is used to read middle nibble data from ROM that addressed by DMA0 ~ DMA2. (2) Write this register with data 05h will clear watch dog timer (WDT) (3) Write this register with data 0Ah will clear RTC counter. |
| DMDH | 1EH | R | xxxx | DMDH.3 | DMDH.2 | DMDH.1 | DMDH.0 | DMDH is used to read high nibble data from ROM that addressed by DMA0 ~ DMA2. |

For example, assume the data of address 356H is 587H.

```
LD A, #3
LD (DMA2), A
LD A, #5
LD (DMA1), A
LD A, #6
LD (DMA0), A ; ROM address = 356H
LD A, (DMDL) ; A register = 7H ; low nibble data of ROM address 356H
LD A, (DMDM) ; A register = 8H; middle nibble data of ROM address 356H
LD A, (DMDH) ; A register = 5H; high nibble data of ROM address 356H
.....
```

5.2 SRAM and I/O Memory Map

TR4P153BT/BF provides 256 nibbles SRAM. SRAM is separated into 8 pages (MAH0~7). Every page has 32 nibbles (with same address, \$20H~\$3FH). This addressing space of SRAM is different from ROM's address.



| Direct Addressing (use MAH) | | Real SRAM Address | SRAM MAP |
|------------------------------|---------|-------------------|---|
| MAH=XH (MAH no effect) | 00H~1FH | | Common I/O port and SFR(special function register) register |
| MAH=0H | 20H~3FH | 00H~1FH | USER SRAM (256x4) |
| MAH=1H | 20H~3FH | 20H~3FH | |
| | | | |
| MAH=6H | 20H~3FH | C0H~DFH | |
| MAH=7H | 20H~3FH | E0H~FFH | |

The addressing space is separated into several pages. Software can select working pages by setting MAH register. Each page contains two blocks and each block contains 32 nibbles. The lower block (00H ~1FH) is used for IO registers and special registers, it's named "common I/O block". This block will not be affected by MAH setting. In any MAH setting, software can access register of this block directly. The higher block (20H~3FH) is used for user SRAM access. MAH register determines current access page of SRAM. The 20H~3FH address (in instructions) determines 32 nibble address in the current page.

The working space shown as below:

| |
|--|
| High 32 nibbles address space (20 ~ 3F H), MAH pointed SRAM space |
| Low 32 nibbles address space (0 ~ 1F H), I/O and special register, "common I/O block", MAH has no effect on this block |

MAH = 0 selects 1st 32 nibbles SRAM

MAH = 1 selects 2nd 32 nibbles SRAM

MAH = 2 selects 3rd 32 nibbles SRAM

...

etc.

MAH can be written by a special instruction "LDMAH" with direct data.

MAH can not be read by MCU. When interrupt happened, MAH data will be stored by hardware and restored by "RETI" command.

5.3 I/O Memory Map

The I/O memory map consists of common I/O, control registers and extended I/O space. Detailed operations are as follows:

5.4 Common I/O and control register

The "common IO block" contains 32 addresses. All registers in this block can be accessed directly by these instructions : LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR. SET, CLR (bit set/clear) can only operate on the address range from 00H to 0FH.

Read common I/O instruction: LD/ADC/SBC/CMP/OR/AND/XOR (Ex. LD A,(n))

Write data to common I/O instruction: LD (n),A

Read and write common I/O instruction : DEC/INC/ADR/RRC/RLC (Ex. DEC (n))

U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|---------------|------|-----|-------|--------|--------|----|----|---|
| STATUS | 00H | R/W | 00xx | TM2IFG | TM1IFG | CF | ZF | ZF : Zero status register CF : Carry status register TM1IFG: Timer 1 interrupt flag 0: no Timer1 interrupt occurred. 1: Timer1 interrupt occurred, it can be cleared by software. |



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| | | | | | | | | |
|-----------------|-----|-----|------|------------------|---------|---------|---------|---|
| | | | | | | | | TM2IFG: Timer 2 interrupt flag 0: no Timer 2 interrupt occurred. 1: Timer2 interrupt occurred, it can be cleared by software. |
| RTC | 01H | R/W | 0000 | RTCFG | F38K | RTCS1 | RTCS0 | <p>RTC will cause an interrupt (\$008h) when in NORMAL mode or GREEN mode. In HALT mode, RTC can wakeup MCU and program will go to wake up vector (\$004h).</p> <p>RTCS1, RTCS0: RTC interrupt period detailed description in Real Time Clock Interrupt section.</p> <p>F38K is valid only when IREN is enabled. F38K = 1, PA1 output 38k clock F38K = 0, PA1 PIN 38K output signal disabled. PA1 keeps low if (option) IRNOR0 disabled. PA1 keeps high when IRNOR0 enabled.</p> <p>RTCFG: RTC overflow flag 0: RTC overflow not occurred. 1: RTC overflow occurred, it can be cleared by software.</p> |
| IOC_PA | 02H | R/W | 0000 | X | IOCA2 | IOCA1 | IOCA0 | Port PA0~PA2 input/output direction : 1: set port as output port individually 0: set port as input port individually PA3 is input only. |
| DATA_PA | 03H | R/W | xxxx | DPA3 (Read only) | DPA2 | DPA1 | DPA0 | Read data from PA0~PA3 PIN or write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register) |
| Reserved | 04H | x | xxxx | x | x | x | x | reserved |
| IOC_PB | 05H | R/W | 0000 | IOCB3 | IOCB2 | IOCB1 | IOCB0 | Port PB0~PB3 input/output direction : 1: set port as output port individually 0: set port as input port individually |
| DATA_PB | 06H | R/W | xxxx | DPB3 | DPB2 | DPB1 | DPB0 | Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register) |
| USER1 | 07H | R/W | xxxx | USER1.3 | USER1.2 | USER1.1 | USER1.0 | General purpose user RAM |
| TMCTL | 08H | R/W | 0000 | TM2EN | TM1EN | TM1SCK | TM1ALD | <p>TM1ALD: Timer 1 auto load control 0 : Timer 1 auto load function turned off 1 : Timer 1 auto load function turned on</p> <p>TM1SCK:Timer1 clock source selection 0: internal clock (frequency selected by SCALER1 register) 1: external clock (from PA2 pin) IOCA2 must be set to 0.</p> <p>TM1EN: Timer 1 enable control bit 0 : Timer 1 disabled 1 : Timer 1 enabled</p> <p>TM2EN: Timer 2 enable control bit 0 : Timer 2 disabled 1 : Timer 2 enabled</p> |



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TR4P153BT/BF

| SYS0 | 09H | R/W | 0000 | TM2MSK | TM1MSK | ENINT | PWMO | <p>Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction</p> <p>PWMO: PWM signal output to PA2 pin 0 : PA2 pin is I/O pin 1 : PA2 pin is PWM output pin (The frequency of PWM is controlled by TM1OUT and TM1ALD if PWMO=1) ENINT: Global interrupt enable 0 : global interrupt disabled 1 : global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM1MSK : Timer 1 interrupt mask 0 : Timer 1 interrupt masked (Timer1 interrupt disabled). 1 : Timer 1 interrupt unmasked (Timer1 interrupt enabled). TM2MSK : Timer 2 interrupt mask 0 : Timer 2 interrupt masked (Timer2 interrupt disabled). 1 : Timer 2 interrupt un-masked (Timer2 interrupt enabled).</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|--------|--------|-----------|--------------------|--------------------|--------------------|--------------------|--|--------|--------|--------|-------|---|---|---|----------|---|---|---|-----------|---|---|---|----------|---|---|---|----------|---|---|---|----------|---|---|---|---------|---|---|---|---------|---|---|---|---------|
| TIM1 | 0AH | R/W | 0000 | TIM1.3 (TIM1.7) | TIM1.2 (TIM1.6) | TIM1.1 (TIM1.5) | TIM1.0 (TIM1.4) | <p>TIM1.7~TIM1.0: 8 bit TIMER 1 counter value, read or write must follow fixed sequence as shown below: (1) Write: write low nibble first, and then write high nibble. (2) Read: read low nibble first, and then read high nibble.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TIM2 | 0BH | R/W | 0000 | TIM2.3 (TIM2.7) | TIM2.2 (TIM2.6) | TIM2.1 (TIM2.5) | TIM2.0 (TIM2.4) | <p>TIM2.7~TIM2.0: 8 bit TIMER 2 counter value, read or write must follow fixed sequence as shown below: (1) Write: write low nibble first, and then write high nibble. (2) Read: read low nibble first, and then read high nibble.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| IOC_PD | 0CH | R/W | 0000 | IOCD3 | IOCD2 | IOCD1 | IOCD0 | <p>Port D input/output direction select 1: set port as output port individually 0: set port as input port individually</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DATA_PD | 0DH | R/W | xxxx | DPD3 | DPD2 | DPD1 | DPD0 | <p>Read port D data from PD0~PD3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register)</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SCALER1 | 0EH | R/W | 0000 | TM1OUT | T1DIV2 | T1DIV1 | T1DIV0 | <p>T1DIV2~0: The pre-scaler of Timer 1. Timer 1 clock source definition table: (FMCK = MCU operating clock)</p> <table border="1"> <thead> <tr> <th>T1DIV2</th> <th>T1DIV1</th> <th>T1DIV0</th> <th>TM1CK</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>FMCK/256</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>FMCK /128</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>FMCK /64</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>FMCK /32</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>FMCK /16</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>FMCK /8</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>FMCK /4</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>FMCK /2</td> </tr> </tbody> </table> <p>TM1OUT: Select PA2 as "Timer 1 toggle signal output" (PWMO must be 0 to enable this function). 0 : Disabled, PA2 port is I/O function 1 : Enable PA2 as Timer 1 toggle output (BZ).</p> | T1DIV2 | T1DIV1 | T1DIV0 | TM1CK | 0 | 0 | 0 | FMCK/256 | 0 | 0 | 1 | FMCK /128 | 0 | 1 | 0 | FMCK /64 | 0 | 1 | 1 | FMCK /32 | 1 | 0 | 0 | FMCK /16 | 1 | 0 | 1 | FMCK /8 | 1 | 1 | 0 | FMCK /4 | 1 | 1 | 1 | FMCK /2 |
| T1DIV2 | T1DIV1 | T1DIV0 | TM1CK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | FMCK/256 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | FMCK /128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | FMCK /64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | FMCK /32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | FMCK /16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | FMCK /8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | FMCK /4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | FMCK /2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |



| USER2 | 0FH | R/W | xxxx | USER2.3 | USER2.2 | USER2.1 | USER2.0 | General purpose user RAM | | | |
|---------------------------------|---------|----------------------------------|------|--|---------|---------|---------|---|--------|--|-----------------------|
| MDCTL | 10H | W | 1100 | MD1 | MD0 | X | X | MCU operation mode selection table | | | |
| | | | | | | | | MD1 | MD0 | MCU MODE | |
| | | | | | | | | 0 | 0 | Into HALT mode (or use HALT instruction) | |
| | | | | | | | | 0 | 1 | Enters NORMAL mode | |
| | | | | | | | | 1 | 0 | Enters GREEN mode | |
| 1 | 1 | reserved, do not set this value. | | | | | | | | | |
| Reserved | 11H~17H | | | | | | | Reserved | | | |
| DMA0 | 18H | R/W | xxxx | DMA0.3 | DMA0.2 | DMA0.1 | DMA0.0 | DMA0~DMA2(exclude DMA2.3) build a 11 bit addressing space for read ROM data. DMA0 is the lowest nibble address, DMA2 is the highest nibble address. DMA2.3: It's a user usable register only, it's useless for address setting. | | | |
| DMA1 | 19H | R/W | xxxx | DMA1.3 | DMA1.2 | DMA1.1 | DMA1.0 | | | | |
| DMA2 | 1AH | R/W | xxxx | DMA2.3 | DMA2.2 | DMA2.1 | DMA2.0 | | | | |
| Reserved | 1BH | x | xxxx | x | x | x | x | Reserved | | | |
| DMDL | 1CH | R | xxxx | DMDL.3 | DMDL.2 | DMDL.1 | DMDL.0 | DMDL is used to read low nibble data from ROM that addressed by DMA0 ~ DMA2. | | | |
| DMDM | 1DH | R/W | xxxx | DMDM.3 | DMDM.2 | DMDM.1 | DMDM.0 | (1) DMDM is used to read middle nibble data from ROM that addressed by DMA0 ~ DMA2. (2) Write this register with data 05h will clear watch dog timer (WDT) (3) Write this register with data 0Ah will clear RTC counter. | | | |
| DMDH | 1EH | R | xxxx | DMDH.3 | DMDH.2 | DMDH.1 | DMDH.0 | DMDH is used to read high nibble data from ROM that addressed by DMA0 ~ DMA2. | | | |
| SCALER2 | 1FH | R/W | 0000 | TM2ALD | T2DIV2 | T2DIV1 | T2DIV0 | T2DIV2~0: The pre-scaler of Timer 2 (F _{MCK} = MCU operating clock) | | | |
| | | | | | | | | T2DIV2 | T2DIV1 | T2DIV0 | TM2CK |
| | | | | | | | | 0 | 0 | 0 | F _{MCK} /256 |
| | | | | | | | | 0 | 0 | 1 | F _{MCK} /128 |
| | | | | | | | | 0 | 1 | 0 | F _{MCK} /64 |
| | | | | | | | | 0 | 1 | 1 | F _{MCK} /32 |
| | | | | | | | | 1 | 0 | 0 | F _{MCK} /16 |
| | | | | | | | | 1 | 0 | 1 | F _{MCK} /8 |
| | | | | | | | | 1 | 1 | 0 | F _{MCK} /4 |
| | | | | | | | | 1 | 1 | 1 | F _{MCK} /2 |
| | | | | TM2ALD: Timer 2 auto load control 0 : Timer 2 auto load function turned off 1 : Timer 2 auto load function turned on | | | | | | | |
| USER SRAM 256 nibbles | 20H~3FH | R/W | XXXX | SRAM.3 | SRAM.2 | SRAM.1 | SRAM.0 | User SRAM, MAH = 0~7H, use MAH to change SRAM page. | | | |

5.5 Extended I/O

TR4P153BT/BF is provided one special instruction "LD **EXIO**(n), A", where n = 00H ~ 0FH" to obtain the 16 extra I/O registers. These registers are used for the I/O port pull up or down resistors control and can be accessed by two "LD" data transfer instruction only.

For example, to enable the pull up resistor of port A, the program should be as below:

```
LD A, #FH
LD EXIO(00H), A
```



U: unchanged X: unknown value R/W: readable & writeable R: readable only W: writeable only

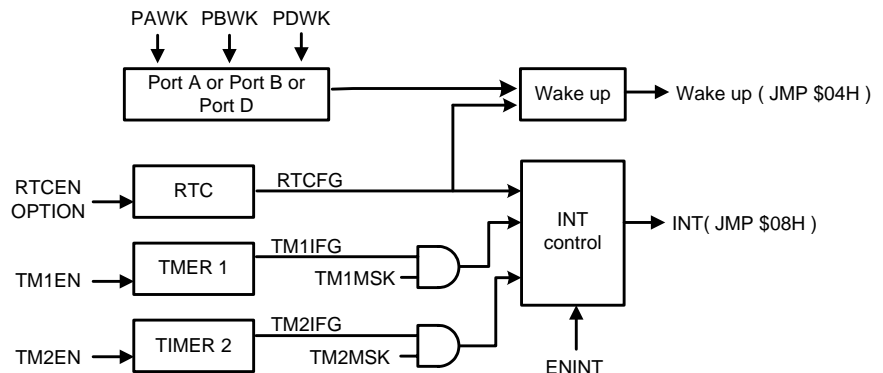
| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|----------|-------------|-----|-------|--------|--------|--------|--------|--|
| PAPU | 00H | W | 0000 | PAPU.3 | PAPU.2 | PAPU.1 | PAPU.0 | PA2~PA0 pull up 100K ohm resistor PA3 pull up 60K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled |
| PAPL | 01H | W | 0000 | PAPL.3 | PAPL.2 | PAPL.1 | PAPL.0 | Port A pull down 100K ohm resistor 0: Port A pull down resistor disabled 1: Port A pull down resistor enabled |
| PBPU | 02H | W | 0000 | PBPU.3 | PBPU.2 | PBPU.1 | PBPU.0 | Port B pull up 100K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled |
| PBPL | 03H | W | 0000 | PBPL.3 | PBPL.2 | PBPL.1 | PBPL.0 | Port B pull down 100K ohm resistor 0: Port B pull down resistor disabled 1: Port B pull down resistor enabled |
| PDPU | 04H | W | 0000 | PDPU.3 | PDPU.2 | PDPU.1 | PDPU.0 | Port D pull up 100K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled |
| PDPL | 05H | W | 0000 | PDPL.3 | PDPL.2 | PDPL.1 | PDPL.0 | Port D pull down 100K ohm resistor 0: Port D pull down resistor disabled 1: Port D pull down resistor enabled |
| PAWK | 06H | W | 0000 | PAWK.3 | PAWK.2 | PAWK.1 | PAWK.0 | Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled |
| PBWK | 07H | W | 0000 | PBWK.3 | PBWK.2 | PBWK.1 | PBWK.0 | Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled |
| PDWK | 08H | W | 0000 | PDWK.3 | PDWK.2 | PDWK.1 | PDWK.0 | Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled |
| Reserved | 09H~ 0FH | | | | | | | Reserved |

5.6 Interrupt Processing

Interrupt vector address definition

| Event | Vector Address |
|------------------------|----------------|
| RESET | 00H |
| System reserved | 02H |
| WAKE UP | 04H |
| System reserved | 06H |
| Timer1(PWM)/Timer2/RTC | 08H |

When any interrupt request flag (RTCFG, TM1IFG, TM2IFG) is set to "1". Interrupt would happen or not. It depends on the interrupt mask (TM1MSK, TM2MSK) and global interrupt enable (ENINT) setting. If interrupt mask set to "1" and global interrupt enable set to "1", Interrupt will be accepted on the next clock after these interrupt request flag set to "1". The following four procedures are done in one clock cycle by hardware as shown below:





1. Program Counter, MAH, PCDH and C/Z will be stored in special hardware registers.
2. Program counter will be changed to the corresponding interrupt vector address.
3. The global interrupt enable register ENINT is automatically stored in special hardware register by hardware.
4. ENINT is cleared to "0", so interrupt control circuit will be disabled by hardware to avoid unwanted interrupt in interrupt handling routine.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware as shown below:

1. Restore the Program Counter, MAH, PCDH and C/Z, which were stored when interrupt happened.
2. The global interrupt enable register ENINT is restore from special register which is stored before interrupt by hardware automatically. This will allow subsequent Interrupt to happen.

The corresponding interrupt request flag must be cleared to "0" by software, before executing RETI instruction. Otherwise, the interrupt procedure will be executed again.

In normal case, if the interrupt accepted by this chip and program jumps into interrupt service routing, the register ENINT must be "1". It will not accept the interrupt when register ENINT is equal to "0". But when clearing ENINT instruction (disable interrupt) is executed, and interrupt happened at next cycle, then the interrupt may still be accepted. This will sometimes causes fault. To avoid this, one "NOP" instruction right after "ENINT clear" is needed.

Notice: Be very careful on the next instruction right after interrupt disabled (ENINT = 0) or timer interrupt mask(TM1MSK=0 or TM2MSK=0). If this instruction contains global variable that is used in both main program and interrupt routine, then it may not work properly (as described above). To ensure the correct operation, one "NOP" instruction right after clearing register ENINT or TM1MSK,TM2MSK (set to zero) is needed.

Example: (1) before modified

```

.....
CLR #1, (SYS0) ; clear ENINT to zero ( or TM1MSK=0 or TM2MSK=0 )
SET #1,(XXX)  ; XXX is global variable, interrupt may be accepted at this line and jump to
                ; interrupt service routing after this instruction (SET #1(xx) ) executed
                ; successfully. This will be incorrect.

```

(2) after modified

```

.....
CLR #1, (SYS0) ; clear ENINT to zero ( or TM1MSK=0 or TM2MSK=0 )
NOP            ; inserted one "NOP" instruction, and ensure next instruction
                ; SET #1,(XX) is executed after interrupt disabled ( ENINT=0 )
SET #1,(XXX)  ; XXX is global variable.

```

5.7 Operation mode

TR4P153BT/BF is provided 3 different modes for low power consumption management by switching around NORMAL mode, GREEN mode and HALT mode.

Common I/O control register

| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|--------|------|-----|-------|-----|-----|----|----|--------------------------------------|
| MDCTL | 10H | W | 1100 | MD1 | MD0 | X | X | MCU operation mode control register. |

Notice: After reset MD1, MD0 = 11, it's meaningless. Don't write MD1,MD0=11 to this register.

There are three operation modes which are defined at the following table. It can be changed from NORMAL mode to HALT mode or GREEN mode for power saving by setting MD [1:0] of register MDCTL.

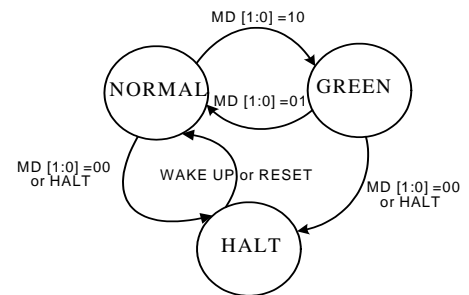


| MD1 | MD0 | MCU MODE | HRCOSC or EXTOSC | LRCOSC | MCU clock (F _{MCK}) |
|-----|-----|---|------------------|---------|---|
| 0 | 0 | into HALT mode, or use HALT instruction | stop | enabled | stop |
| 0 | 1 | into NORMAL mode Notice: The “NOP” instruction must be inserted after this command. See Notice 1 below | enabled | enabled | (1) HRCOSC----- MCU run 8 MIPS / 4 MIPS / 2 MIPS / 1 MIPS by option (2) EXTOSC ----- MCU run F _{xtosc} /2 |
| 1 | 0 | into GREEN mode | stop | enabled | MCU run 114.69KIPS / 57.34KIPS / 28.67KIPS / 14.33KIPS by option |
| 1 | 1 | reserved | - | - | Do not use this value. |

Notice 1 : If MCU running in GREEN mode, the following steps will change MCU from GREEN mode to NORMAL mode(MD1,MD0 = 0 1). An additional “NOP” instruction must be inserted right after MDCTL setting instruction.

The state diagram of these three MCU operation modes are shown as follows:

1.NORMAL Mode: In NORMAL mode, both high speed RC oscillator (HRCOSC) and low speed RC oscillator (LRCOSC) are running. MCU clock source is come from HRCOSC oscillator. The default operation mode of TR4P153BT/BF is NORMAL mode after reset. User can change operation mode to HALT mode from NORMAL mode by setting MD [1:0] =00 or execute HALT instruction. If in NORMAL mode, MCU can go to GREEN mode by setting MD[1:0]=10.



2.HALT Mode: In HALT mode, main oscillator HRCOSC is stopped. So the MCU operation is also stopped. But LRCOSC oscillator may still running(if enabled). User can't change the operation mode when in HALT mode. Chip will go back to NORMAL mode when RTC interrupt, I/O wake up or reset occurred. For detail HALT mode description, please refer to section 5.8.

3.GREEN Mode: In GREEN mode, only LRCOSC oscillator keep running, HRCOSC oscillator is stop. MCU uses LRCOSC as system clock source. It's very low speed for low power consumption application. MCU may get to NORMAL mode by setting MD[1:0]=01 if operation speed is not enough. It's also allowed to enter HALT mode by setting MD[1:0]=00 or execute HALT instruction.

5.8 Halt Mode & Wake up

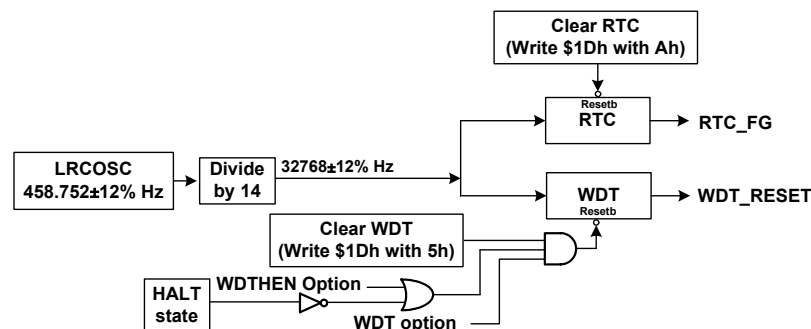
The MCU operation may be switched to HALT mode (MCU operation clock and HRCOSC stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA0~PA3, PB0~PB3 and PD0~PD3 are provided with wake up function on rising edge or falling edge. When wake up condition occurred, program will start from \$004H address after stable clock delay (CKstable3 or CKstable4). “system reset” signal will release HALT state and execute reset procedure. SRAM will keep their previous data without change in HALT mode.

Notice: The register PWMO, ENINT, TMIMSK and TM2MSK will be cleared after wake up by hardware, so re-assign those registers are necessary if interrupt is needed after wakeup.



5.9 Watch Dog Timer Reset (WDT)

The watch dog timer (WDT) is used to reset chip when unexpected execution sequence caused, avoiding dead lock of MCU program. This timer can be enabled or disabled by option only. WDT will not have any action when WDT option disabled. Software shall run an "clear watch dog timer" (write data 5 to register \$1D) instruction before WDT time out if WDT option is enabled. Hardware will generate a reset signal to reset whole system when WDT overflow. It's provided with four kinds of time-out period (0.125sec~1sec) by WDS1 and WDS0 option. The clock source of WDT comes from internal LRCOSC oscillator. If WDT function is enabled by WDT option, the WDT can work in both HALT mode and NORMAL mode, or only works in NORMAL mode (WDT disabled in HALT mode) by WDTTHEN option.



WDT period definition by option

| WDS1 | WDS0 | WDT Period |
|------|------|---------------|
| 0 | 0 | 0.125±12% Sec |
| 0 | 1 | 0.25±12% Sec |
| 1 | 0 | 0.5±12% Sec |
| 1 | 1 | 1.0±12% Sec |

WDT will be reset when wake up from HALT mode, power on reset, or cleared by software. Reset watch dog timer sequence is as below:

```
LD    A, #05H
LD    (1DH), A ; clear watch dog timer
```

Notice: For good system reliability, It's strongly recommended that, do not use more than one "reset watch dog" instruction in whole program.

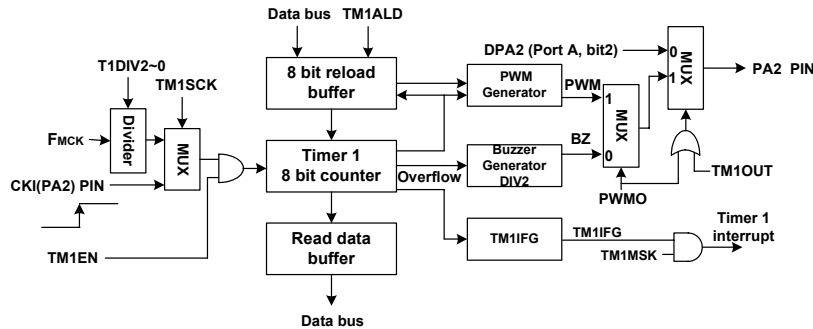
5.10 Programable 8 bits Timer/Counter--- Timer1

5.10.1 Timer1

The Timer 1 is an 8 bit up timer which can be configured as programmable frequency generator(PFD), PWM generator or event counter. The interrupt interval is generated by selected clock source and specific different values of Timer 1. The content of Timer 1 is readable and writable by user program.

PA2 pin function definition table

| PWMO register | TM1OUT register | PA2 output pin |
|---------------|-----------------|----------------|
| 0 | 0 | DPA2 register |
| 0 | 1 | PFD generator |
| 1 | X | PWM generator |



| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|---------------|------|-----|-------|------------------------|------------------------|------------------------|------------------------|--|
| STATUS | 00H | R/W | 00xx | TM2IFG | TM1IFG | CF | ZF | TM1IFG: Timer 1 interrupt flag 0: no Timer 1 interrupt occurred. 1: Timer 1 interrupt occurred, it can be cleared by software. |
| TMCTL | 08H | R/W | 0000 | TM2EN | TM1EN | TM1SCK | TM1ALD | TM1ALD: Timer 1 auto load control 0: Timer 1 auto load function turned off 1: Timer 1 auto load function turned on TM1SCK: Timer 1 clock source selection 0: internal clock (frequency selected by SCALER1 register) 1: external clock (from PA2 pin) IOCA2 must be set to 0. TM1EN: Timer 1 enable control bit 0: Timer 1 disabled 1: Timer 1 enabled |
| SYS0 | 09H | R/W | 0000 | TM2MSK | TM1MSK | ENINT | PWMO | Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction PWMO: PWM signal output to PA2 pin 0: PA2 pin is I/O pin 1: PA2 pin is PWM output pin (The frequency of PWM is controlled by TM1OUT and TM1ALD if PWMO=1) ENINT: Global interrupt enable 0: global interrupt disabled 1: global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM1MSK : Timer 1 interrupt mask 0: Timer 1 interrupt masked (Timer1 interrupt disabled). 1: Timer 1 interrupt unmasked (Timer1 interrupt enabled). |
| TIM1 | 0AH | R/W | 0000 | TIM1.3 (TIM1.7) | TIM1.2 (TIM1.6) | TIM1.1 (TIM1.5) | TIM1.0 (TIM1.4) | TIM1.7~TIM1.0: 8 bit TIMER 1 counter value, read or write must follow fixed sequence as shown below: (1) Write: write low nibble first , and then write high nibble. (2) Read: read low nibble first , and then read high nibble. |



| | | | | | | | | |
|---------|-----|-----|------|--------|--------|--------|--------|---|
| SCALER1 | 0EH | R/W | 0000 | TM1OUT | T1DIV2 | T1DIV1 | T1DIV0 | T1DIV2~0: The pre-scaler of Timer 1. TM1OUT: Select PA2 as "Timer 1 toggle signal output" (PWMO must be 0 to enable this function). 0 : Disabled, PA2 port is I/O function 1 : Enable PA2 as Timer 1 toggle output (BZ). |
|---------|-----|-----|------|--------|--------|--------|--------|---|

The clock source of Timer 1 can come from external PIN CKI(PA2) or internal MCU's clock by option. The event counter would be constructed by selecting external clock CKI as clock source of Timer 1. The counter will react to rising edge of external clock signals at the CKI(PA2) pin.
If internal clock source used, there are 8 kind of clock rate selectable by register T1DIV2~T1DIV0.

Timer 1 clock source table (F_{MCK} = MCU operating clock)

| T1DIV2 | T1DIV1 | T1DIV0 | Timer 1 clock in NORMAL mode (if $F_{MCK} = 8MIPS$) | Timer 1 clock in GREEN mode (if $F_{MCK} = 114.69KIPS$) |
|--------|--------|--------|--|--|
| 0 | 0 | 0 | $F_{MCK} \div 256 = 31.25KHz$ | $F_{MCK} \div 256 = 0.448KHz$ |
| 0 | 0 | 1 | $F_{MCK} \div 128 = 62.5KHz$ | $F_{MCK} \div 128 = 0.896KHz$ |
| 0 | 1 | 0 | $F_{MCK} \div 64 = 125KHz$ | $F_{MCK} \div 64 = 1.792KHz$ |
| 0 | 1 | 1 | $F_{MCK} \div 32 = 250KHz$ | $F_{MCK} \div 32 = 3.584KHz$ |
| 1 | 0 | 0 | $F_{MCK} \div 16 = 500KHz$ | $F_{MCK} \div 16 = 7.168KHz$ |
| 1 | 0 | 1 | $F_{MCK} \div 8 = 1MHz$ | $F_{MCK} \div 8 = 14.336KHz$ |
| 1 | 1 | 0 | $F_{MCK} \div 4 = 2MHz$ | $F_{MCK} \div 4 = 28.672KHz$ |
| 1 | 1 | 1 | $F_{MCK} \div 2 = 4MHz$ | $F_{MCK} \div 2 = 57.345KHz$ |

The Timer 1 interrupt interval time and the content value equation is described as following :

The content value of Timer 1 = **256 - (interrupt interval time \div Timer 1 clock time period)**

Example: If someone wants to get 360us interrupt interval time, and set T1DIV2~T1DIV0=011. Then, Timer 1 clock time period = $1/250k=4us$. So **the content value of Timer 1 = 256 - (360us/4us) = 166 = A6h**

The 8 bits content of Timer 1 can be assigned by register TIM1.7~TIM1.0. To write this 8 bit value, write low nibble data first, then write high nibble data. To read TIM1 data, read low nibble first then read high nibble.

Notice 1: The TIM1 registers must be read or written twice (low nibble first and high nibble later) in sequence. Only one nibble read or write is prohibited.

Notice 2: The TIM1 register can be assigned data either in interrupt routing or in main program. If in main program, register ENINT must be disabled before write or read data to TIM1. After write or read data to/from TM1 high nibble, ENINT can be enabled if needed.

Example : in main program

```

.....
CLR #1, (SYS0) ; ENINT=0, ENINT disabled
NOP           ; added NOP instruction
LD A,#DH     ; setting TIM1 low nibble first
LD (TIM1),A
LD A,#FH     ; setting TIM1 high nibble later
LD (TIM1),A
SET #1,(SYS0) ; ENINT=1, ENINT enabled
.....

```

The auto load function is enabled by setting TM1ALD to 1. This 8 bits data will be reloaded into 8 bits up counter while Timer 1 overflow occurred. The interrupt mask control register (TM1MSK) of Timer 1 is used to inhibit interrupt request for MCU. TM1MSK value will not affect normal Timer 1 operation. Even when TM1MSK is masked, TM1IFG will still be set to 1 when overflow occurred, and Timer 1 still keep running. The global interrupt control register (ENINT) should be set to 1 before Timer 1 start. After setting of these control registers, software can enable Timer 1 counter with register TM1EN set to 1. Then Timer 1 will issue an interrupt request (register TM1IFG=1) when the Timer 1 counts from FFH to 00H.



5.10.2 PWM Generator (use Timer 1)

Timer 1 could be configured as PWM Generator by setting PWMO to 1. In this mode, there are four kinds of operation controlled by register TM1ALD and TM1OUT (TM1ALD and TM1OUT as the frequency control of PWM). The PWM interrupt request will be issued at every rising edge of PA2 (output) signal.

PA2 pin function definition table

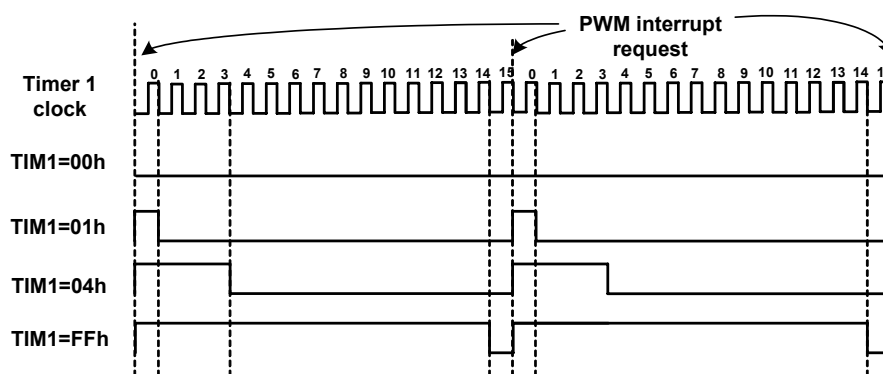
| PWMO register | TM1OUT register | PA2 output pin |
|---------------|-----------------|----------------|
| 0 | 0 | DPA2 register |
| 0 | 1 | PFD generator |
| 1 | X | PWM generator |

The clock source of PWM generator comes from MCU clock (F_{MCK}) that depends on current MCU operation and oscillator mode. So MCU clock (F_{MCK}) may be HRCOSC (8 MIPS, 4 MIPS, 2 MIPS, 1 MIPS) ,LRCOSC (114.69KIPS, 57.34KIPS, 28.67KIPS, 14.33KIPS) or EXTOSC (8 MIPS~0.5 MIPS).

If HRCOSC used as PWM clock source, in NORMAL mode, the max. and min. PWM frequency is as below:

| TM1ALD | TM1OUT | Step | Timer 1 value (TIM1) | Max. PWM(PA2) frequency Set $F_{MCK} = 8 \text{ MIPS}$ $T1DIV2 \sim 0 = 111$ | Min. PWM(PA2) frequency Set $F_{MCK} = 1 \text{ MIPS}$ $T1DIV2 \sim 0 = 000$ |
|--------|--------|------|----------------------|--|--|
| 0 | 0 | 256 | 00h~FFh | $(F_{MCK} \div 2) \div 256 = 15.6K$ | $(F_{MCK} \div 256) \div 256 = 15.25Hz$ |
| 0 | 1 | 64 | 00h~3Fh | $(F_{MCK} \div 2) \div 64 = 62.5K$ | $(F_{MCK} \div 256) \div 64 = 61Hz$ |
| 1 | 0 | 32 | 00h~1Fh | $(F_{MCK} \div 2) \div 32 = 125K$ | $(F_{MCK} \div 256) \div 32 = 122Hz$ |
| 1 | 1 | 16 | 00h~0Fh | $(F_{MCK} \div 2) \div 16 = 250K$ | $(F_{MCK} \div 256) \div 16 = 244Hz$ |

Example: PWM(PA2) output waveform (TM1ALD=1, TM1OUT=1)



5.10.3 Programmable Frequency Divider (PFD)---- (use Timer 1)

Timer 1 can be configured as programmable frequency divider (PFD) by setting TM1OUT to 1 and PWMO to 0, can output single tone signal to BZ (PA2) pin. No interrupt will occur in this mode. If F_{MCK} is 8 MIPS, the frequency of PDF ranges from 61Hz to 2MHz in NORMAL mode, duty cycle 50%, square wave output. It's suitable for driving buzzer or other applications. Timer 1 can be regarded as a programmable frequency divider. Its frequency is selected by register T1DIV2~T1DIV0 and combining the operation of content value of Timer 1.

The clock source of PFD generator comes from MCU clock (F_{MCK}) that depends on current MCU operation and oscillator mode. So MCU clock (F_{MCK}) may be HRCOSC (8 MIPS, 4 MIPS, 2 MIPS, 1 MIPS), LRCOSC (114.69KIPS, 57.34KIPS, 28.67KIPS, 14.33KIPS) or EXTOSC (8 MIPS~0.5 MIPS).



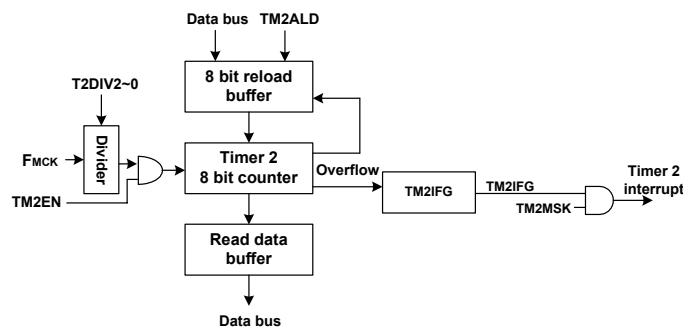


If MCU run 8MIPS, in NORMAL mode, the BZ(PA2) clock output is as below:

| T1DIV2 | T1DIV1 | T1DIV0 | BZ(PA2) clock output |
|--------|--------|--------|---|
| 0 | 0 | 0 | $(F_{MCK} \div 256) \div (1 \sim 256) \div 2 = 0.061\text{KHz} \sim 15.625\text{KHz}$ |
| 0 | 0 | 1 | $(F_{MCK} \div 128) \div (1 \sim 256) \div 2 = 0.122\text{KHz} \sim 31.25\text{KHz}$ |
| 0 | 1 | 0 | $(F_{MCK} \div 64) \div (1 \sim 256) \div 2 = 0.244\text{KHz} \sim 62.5\text{KHz}$ |
| 0 | 1 | 1 | $(F_{MCK} \div 32) \div (1 \sim 256) \div 2 = 0.488\text{KHz} \sim 125\text{KHz}$ |
| 1 | 0 | 0 | $(F_{MCK} \div 16) \div (1 \sim 256) \div 2 = 0.976\text{KHz} \sim 250\text{KHz}$ |
| 1 | 0 | 1 | $(F_{MCK} \div 8) \div (1 \sim 256) \div 2 = 1.952\text{KHz} \sim 500\text{KHz}$ |
| 1 | 1 | 0 | $(F_{MCK} \div 4) \div (1 \sim 256) \div 2 = 3.906\text{KHz} \sim 1000\text{KHz}$ |
| 1 | 1 | 1 | $(F_{MCK} \div 2) \div (1 \sim 256) \div 2 = 7.812\text{KHz} \sim 2000\text{KHz}$ |

5.11 Programable 8 bits Timer2

The Timer 2 is an 8 bit up timer. The interrupt interval is determined by selected clock source and written data of Timer 2. The content of Timer 2 can be read or write by software.



| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|---------------|------|-----|-------|---------------|---------------|---------------|---------------|--|
| STATUS | 00H | R/W | 00xx | TM2IFG | TM1IFG | CF | ZF | TM2IFG: Timer 2 interrupt flag 0: no Timer 2 interrupt occurred. 1: Timer2 interrupt occurred, it can be cleared by software. |
| SYS0 | 09H | R/W | 0000 | TM2MSK | TM1MSK | ENINT | PWMO | Notice: The PWMO, ENINT, TM1MSK and TM2MSK will be cleared by HALT instruction ENINT: Global interrupt enable 0 : global interrupt disabled 1 : global interrupt enabled, (ENINT control the interrupt enable of Timer 1, Timer 2 and RTC) TM2MSK : Timer 2 interrupt mask 0 : Timer 2 interrupt masked (Timer2 interrupt disabled). 1 : Timer 2 interrupt un-masked (Timer2 interrupt enabled). |
| TIM2 | 0BH | R/W | 0000 | TIM2.3 | TIM2.2 | TIM2.1 | TIM2.0 | TIM2.7~TIM2.0: 8 bit TIMER 2 counter |



| | | | | | | | | |
|----------------|-----|-----|------|---------------|---------------|---------------|---------------|--|
| | | | | (TIM2.7) | (TIM2.6) | (TIM2.5) | (TIM2.4) | value, read or write must follow fixed sequence as shown below: (1) Write: write low nibble first , and then write high nibble. (2) Read: read low nibble first , and then read high nibble. |
| SCALER2 | 1FH | R/W | 0000 | TM2ALD | T2DIV2 | T2DIV1 | T2DIV0 | T2DIV2~0: The pre-scaler of Timer 2 TM2ALD: Timer 2 auto load control 0 : Timer 2 auto load function turned off 1 : Timer 2 auto load function turned on |

The clock source of Timer 2 is internal clock. There are 8 kinds of clock rate setting by register T1DIV2~T1DIV0.

TM2CK= Timer 2 clock source ($F_{MCK} = \text{MCU operating clock}$)

| T2DIV2 | T2DIV1 | T2DIV0 | TM2CK |
|--------|--------|--------|-----------------|
| 0 | 0 | 0 | $F_{MCK} / 256$ |
| 0 | 0 | 1 | $F_{MCK} / 128$ |
| 0 | 1 | 0 | $F_{MCK} / 64$ |
| 0 | 1 | 1 | $F_{MCK} / 32$ |
| 1 | 0 | 0 | $F_{MCK} / 16$ |
| 1 | 0 | 1 | $F_{MCK} / 8$ |
| 1 | 1 | 0 | $F_{MCK} / 4$ |
| 1 | 1 | 1 | $F_{MCK} / 2$ |

The 8 bits content of Timer 2 can be assigned by register TIM2.7~TIM2.0. To write this 8 bit value, write low nibble first and then high nibble. To read TIM2.7~TIM2.0, read low nibble first then read high nibble. When TM2ALD is set to 1, this 8 bits data will be reloaded into 8 bits up counter when overflow occurs.

The interrupt mask control register (TM2MSK) of Timer 2 is used to inhibit interrupt request for MCU. TM2MSK value will not affect normal Timer 2 operation. Even when TM2MSK is masked, TM1IFG will still be set to 1 when timer overflow, and Timer 2 still keep running. The global interrupt control register (ENINT) should

be set to 1 before Timer 2 start. After setting of these control registers, software can enable Timer 2 counter with register TM2EN set to 1. Then Timer 2 will issue an interrupt request (register TM2IFG=1) when the Timer 2 counts from FFH to 00H.

Notice 1: The TIM2 registers must be read or written twice (low nibble first and high nibble later) in sequence. Only one nibble read or write is prohibited.

Notice 2: The TIM2 register can be assigned data either in interrupt routing or in main program. If in main program, register ENINT must be disabled before write or read data to TIM2. After write or read data to/from TM2 high nibble, ENINT can be enabled if needed.

Example : in main program

```

.....
CLR #1, (SYS0) ; ENINT=0 ENINT disabled
NOP           ; added NOP instruction
LD A,#DH     ; setting TIM2 low nibble first
LD (TIM2),A
LD A,#FH     ; setting TIM2 high nibble later
LD (TIM2),A
SET #1,(SYS0) ; ENINT=1 ENINT enabled

```

5.12 Real time clock interrupt (RTC)

| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|-------------|------|-----|-------|---------------|---------------|---------------|---------------|--|
| RTC | 01H | R/W | 0000 | RTCFG | F38K | RTCS1 | RTCS0 | RTCS1, RTCS0: RTC interrupt period selection table as below. RTCFG: RTC overflow flag 0: no RTC time out occurred. 1: RTC time out occurred, it can be cleared by software. |
| DMDM | 1DH | R/W | xxxx | DMDM.3 | DMDM.2 | DMDM.1 | DMDM.0 | Writing this register with data 0Ah will clear RTC counter value. |

RTC function is enabled by RTCEN option. If RTCEN option is enabled, It will keep running at NORMAL and HALT mode. There are two different interrupt jump address supported after RTC overflow occurred.



If MCU operates in NORMAL/GREEN mode, it will jump to address \$008 after RTC overflow occurred. If MCU is in HALT mode, RTC overflow will wakeup chip and jump to address \$004. The RTCFG flag is set every 0.125sec~1sec (or 15.625ms ~ 125ms, by setting RTCS1 and RTCS0 register and SPUP option) as below:

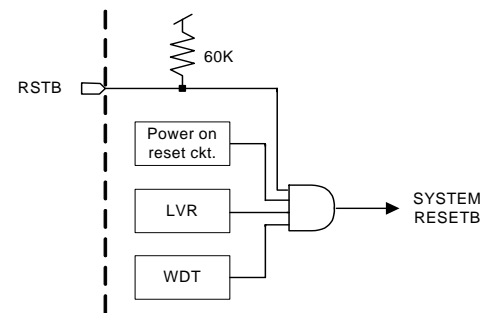
RTCS1,RTCS0: RTC interrupt period selection

| RTCS1 | RTCS0 | RTC Period | |
|-------|-------|---------------------|----------------------|
| | | SPUP option enabled | SPUP option disabled |
| 0 | 0 | 0.125±12% Sec | 15.625±12% ms |
| 0 | 1 | 0.25±12% Sec | 31.25±12% ms |
| 1 | 0 | 0.5 ±12% Sec | 62.5 ±12% ms |
| 1 | 1 | 1.0 ±12% Sec | 125 ±12% ms |

The RTC period can be pre-divided by 8 if SPUP option disabled, and RTCFG flag will be cleared by software. This RTC timer can be used in applications that required to wakeup periodically in HALT mode. The RTC clock source is come from LRCOSC oscillator and the frequency is 458.752KHZ±12%. Besides, RTC counter value also support clear function by writing "0Ah" data to register DMDM (\$1DH).

5.13 Reset

The actual system reset of this chip combines with four signals, which are power on reset, low voltage reset (LVR), external RSTB pin and WDT overflow reset. A dedicated RSTB pin (shared with PA3) can be used to reset TR4P153BT/BF externally. This pin has internal 60K ohm pull up resistor. MCU will go to NORMAL mode when RSTB occurred in HALT mode.



5.14 Low Voltage Reset

When VDD power is applied to the chip, the low voltage RSTB default is enabled initially, it will be disabled when in HALT mode. The internal system reset will be generated if VDD is lower than VLVR.

5.15 System Clock Oscillator

The TR4P153BT/BF provides an internal high speed RC oscillator (HRCOSC) with precision frequency of deviation under ±2%, VDD from 2.0V to 5.5V and temperature from -40 to +85 . An internal low speed RC oscillator (LRCOSC) and an external X'tal oscillator or ceramic resonator (EXTOSC) are provided also. This chip is a dual clock MCU system. In NORMAL mode, MCU operating clock (F_{MCK}) comes from HRCOSC or EXTOSC. In GREEN mode, clock source come from LRCOSC.

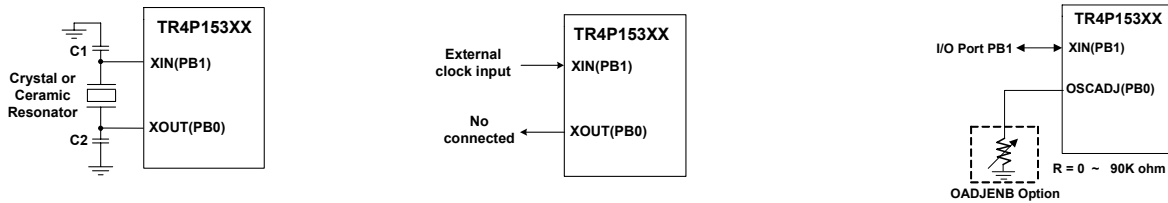
Condition VDD=2.0V~5.5V

| TYPE | OSC frequency | MCU clock (F _{MCK}) | MCU operation mode |
|--------|---|---|---|
| HRCOSC | (1) 32MHz ±2% | F _{HRCOSC} /4, /8, /16, /32 (MCU run 8 MIPS/4 MIPS/2 MIPS/1 MIPS by option) | NORMAL mode |
| | (2) 32MHz -16%~+10% by PB0/OSCADJ pin | | |
| | (3) 32MHz -2%, +2%, -4%, +4% by option | | |
| EXTOSC | 1MHz~16MHz | F _{XTOSC} / 2 , F _{XTOSC} / 4, F _{XTOSC} / 8, F _{XTOSC} / 16 | NORMAL mode |
| LRCOSC | 458.752KHZ±12% | F _{LRCOSC} /4, /8, /16, /32 (MCU run 114.69KIPS /57.34KIPS /28.67KIPS /14.33KIPS by option) | GREEN mode (low power consumption) |

The system clock can be stopped by using HALT command. Once stopped, only wake-up triggering inputs (PA0~PA3, PB0~3 or PD0~PD3), RSTB (if PA3 set as RSTB by option) or RTC overflow can re-start oscillator. Such oscillator will do 'stable check' before release control to software. In order to make system stable, the stable clock delay must be placed between oscillator starting and first instruction of user software. Refer to table on page 5.



EXTOSC: External X'tal oscillator, XIN and XOUT are shared with PB1 and PB0 by option. An external ceramic resonator or crystal of 1MHz~16MHz can be used for MCU clock source. It can be driven by external clock in this mode. In such case, no crystal or resonator is needed. The connection is as follows:
(Cap. C1 and C2 use 20P)



HRCOSC: Internal high speed RC oscillator, the frequency of this oscillator can be adjusted by external OSCADJ (PB0) pin which is selected by option if need. When OSCADJ pin is used for frequency adjust, it must be connected to a resistor and then serial to VSS. The recommended resistor value is from 0 ohm to 90K ohm and the frequency range built around 32MHz -16% ~ +10%. There is one measurement data shown below:

| OSCADJ PIN resistor (KΩ) | 0K | 10K | 20K | 30K | 43K | 51K | 62K | 75K | 82K | 91K |
|----------------------------|------|-------|-----|-------|-------|-------|------|--------|--------|------|
| HRCOSC frequency deviation | -19% | -6.5% | 0% | +4.5% | +7.5% | +8.8% | +10% | +11.8% | +12.2% | +13% |

Note: This data is only for reference. It has some frequency deviation due to process variation, temperature and operating voltage.

There is another frequency adjustment method on HRCOSC. Using IADJENB, ADJ1, and ADJ0 option, the frequency of 32MHz can shift +2%, -2%, +4% or -4% four kinds of frequency deviation. Special care must be taken by user when this method is applied, the device would not guarantee frequency deviation range. These four kinds of frequency deviation is only reference value.

5.16 I/O Port

TR4P153BT/BF provides totally 11 I/O ports and one input port. There are three bi-direction I/O ports, Port A, Port B, and Port D. Input and output direction is controlled by IOC_PA, IOC_PB and IOC_PD. PA3 is input pin only. All I/O are provided with wake up and pull down/up resistor function by control registers.

5.16.1 PortA /PortB (input/output)

Common I/O

| Symbol | Addr | R/W | RSTB | D3 | D2 | D1 | D0 | Description |
|---------|------|-----|------|---------------------|-------|-------|-------|---|
| IOC_PA | 02H | R/W | 0000 | X | IOCA2 | IOCA1 | IOCA0 | Port A input/output direction select 1: set port A as output port individually 0: set port A as input port individually |
| DATA_PA | 03H | R/W | xxxx | DPA3 (Read only) | DPA2 | DPA1 | DPA0 | Read data from PA0~PA3 PIN or write data to PA0~PA2 PIN (I/O direction is selected by IOC_PA register) |
| IOC_PB | 05H | R/W | 0000 | IOCB3 | IOCB2 | IOCB1 | IOCB0 | Port B input/output direction select 1: set port B as output port individually 0: set port B as input port individually |
| DATA_PB | 06H | R/W | xxxx | DPB3 | DPB2 | DPB1 | DPB0 | Read data from PB0~PB3 port or write data to PB0~PB3 (I/O direction is defined by IOC_PB register) |

Extend I/O

| Symbol | Addr | R/W | RSTB | D3 | D2 | D1 | D0 | Description |
|--------|------|-----|------|----|----|----|----|-------------|
|--------|------|-----|------|----|----|----|----|-------------|



| | | | | | | | | |
|-------------|-----|---|------|---------------|---------------|---------------|---------------|--|
| PAPU | 00H | W | 0000 | PAPU.3 | PAPU.2 | PAPU.1 | PAPU.0 | PA2~PA0 pull up 100K ohm resistor PA3 pull up 60K ohm resistor 0: Port A pull up resistor disabled 1: Port A pull up resistor enabled |
| PAPL | 01H | W | 0000 | PAPL.3 | PAPL.2 | PAPL.1 | PAPL.0 | Port A pull down 100K ohm resistor 0: Port A pull down resistor disabled 1: Port A pull down resistor enabled |
| PBPU | 02H | W | 0000 | PBPU.3 | PBPU.2 | PBPU.1 | PBPU.0 | Port B pull up 100K ohm resistor 0: Port B pull up resistor disabled 1: Port B pull up resistor enabled |
| PBPL | 03H | W | 0000 | PBPL.3 | PBPL.2 | PBPL.1 | PBPL.0 | Port B pull down 100K ohm resistor 0: Port B pull down resistor disabled 1: Port B pull down resistor enabled |
| PAWK | 06H | W | 0000 | PAWK.3 | PAWK.2 | PAWK.1 | PAWK.0 | Port A wake up enable control 0: Port A wake up disabled 1: Port A wake up enabled |
| PBWK | 07H | W | 0000 | PBWK.3 | PBWK.2 | PBWK.1 | PBWK.0 | Port B wake up enable control 0: Port B wake up disabled 1: Port B wake up enabled |

The Port A and Port B are 4-bit I/O port. Each bit (pin) can be individually set as input port or output port except PA3. In output mode, data can be written to external pin. In output mode, data read will read internal register data not external pin voltage. Built-in pull-up/down resistor will be disabled when in output mode. In input mode, Port A and Port B data are read voltage from external pin. These pins can have pull-up/down resistor 100K or not. They are selected by PAPU, PAPL, PBPU, PBPL registers. The pull up resistor of PA3 isn't 100k, it's 60K ohm only.

Each pin of Port A and Port B can be selected with wake up function or not by register PAWK or PBWK. In HALT mode, If Port A or Port B wake-up function is enabled. Any rising or falling signal on these selected ports will wake up system and turn on HRCOSC or EXTOSC oscillator simultaneously. Program counter of MCU will jump to address 04H to run wake up program.

When Port A and Port B are selected as wake-up enabled, and system enters HALT by HALT instruction. Then, these ports will enter input mode automatically even if they are set as output ports previously. This function is not provided for Port D and PA3.

PA1 is provided with 38KHz modulator

I/O port PA1 can be used as 38KHz modulator output. This function is enabled by **F38K** modulator option. PA1 pin will output 38KHz clock signal when F38K set to 1 (PA1 always as output port when IREN option enabled). If register F38K set to 0, PA1 output keeps low or high depend on option IRNOR0. See below for detail. If this 38K modulator option is disabled, PA1 will be changed to normal I/O port.

| No. | IRNOR0 option | F38K register | PA1 output pin |
|-----|---------------|---------------|-----------------|
| 1 | disabled | 0 | low |
| 2 | disabled | 1 | 38k square wave |
| 3 | enabled | 0 | high |
| 4 | enabled | 1 | 38k square wave |

This 38KHz modulator has several clock sources under different modes as below:

| MCU mode | NORMAL mode | | GREEN mode |
|---------------|---|--|---|
| Clock source | Use internal HRCOSC | Use external X'tal oscillator Use 16MHz X'TAL is a must | Use internal LRCOSC |
| 38K frequency | $F_{HRCOSC} / 840 = 38.09 \pm 2\% \text{KHz}$ | $F_{XTOSC} = 16\text{Mhz} / 420 = 38.09 \text{KHz}$ | $F_{LRCOSC} / 12 = 38.23 \pm 12\% \text{KHz}$ |



| Symbol | Addr | R/W | Reset | D3 | D2 | D1 | D0 | Description |
|--------|------|-----|-------|--------|------|-------|-------|--|
| RTC | 01H | R/W | 0000 | RTCFCG | F38K | RTCS1 | RTCS0 | F38K is valid only when IREN is enabled. F38K = 1, PA1 output 38k clock F38K = 0, PA1 PIN 38K output signal disabled. PA1 keeps low if (option) IRNOR0 disabled. PA1 keeps high when IRNOR0 enabled. |

PA2 is shared with PWM/CKI/BZ functions by option.

PA3 is an input pin only, with pull up 60K, pull down resistor 100K ohm. It also provides level-change-wakeup function. It's shared with external reset pin (RSTB) pin by option, and VPP pin (VPP is for programming only).

PB0 is shared with XOUT/OSCADJ by option and PB1 is shared with XIN pin by option. XIN and XOUT PIN can be connected to external crystal to replace internal oscillator HRCOSC. Once XTENB option is enabled, the pull up/down control registers and I/O direction registers of these two PINs will be disabled.

PB2 is shared with output of Op Amp by option.

5.16.2 Port D (input/output)

| Symbol | Addr | R/W | RSTB | D3 | D2 | D1 | D0 | Description |
|---------|------|-----|------|-------|-------|-------|-------|---|
| IOC_PD | 0CH | R/W | 0000 | IOCD3 | IOCD2 | IOCD1 | IOCD0 | Port D input/output direction select 1: set port D as output port individually 0: set port D as input port individually |
| DATA_PD | 0DH | R/W | xxxx | DPD3 | DPD2 | DPD1 | DPD0 | Read port D data from PD0~PD3 port or write data to PD0~PD3 (I/O direction is defined by IOC_PD register) |

Extend I/O

| Symbol | Addr | R/W | RSTB | D3 | D2 | D1 | D0 | Description |
|--------|------|-----|------|--------|--------|--------|--------|---|
| PDPU | 04H | W | 0000 | PDPU.3 | PDPU.2 | PDPU.1 | PDPU.0 | Port D pull up 100K ohm resistor 0: Port D pull up resistor disabled 1: Port D pull up resistor enabled |
| PDPL | 05H | W | 0000 | PDPL.3 | PDPL.2 | PDPL.1 | PDPL.0 | Port D pull down 100K ohm resistor 0: Port D pull down resistor disabled 1: Port D pull down resistor enabled |
| PDWK | 08H | W | 0000 | PDWK.3 | PDWK.2 | PDWK.1 | PDWK.0 | Port D wake up enable control 0: Port D wake up disabled 1: Port D wake up enabled |

IOC_PD register defines the input/output selection of PD0~PD3.

PDWK register defines wake up function of PD0~PD3.

PDPU/PDPL defines the existence of 100K pull up/down resistor in input mode, just like Port A or Port B.

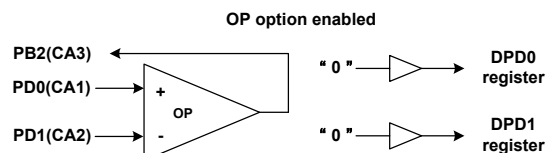
Notice: If Port D pins are wakeup-enabled and is set as output port by software, and if system enters HALT mode, it will not change to input automatically (as port A and port B). It will keep as output.

Only Port A and Port B is provided with this function.

PD0, PD1, PB2 are shared with input/output of OP Amp.

There is one OP Amp in TR4P153BT/BF. The input/output pin of this OP Amp are shared with PD0, PD1 and PB2 pin by option. If OP Amp is enabled, the register DPD0 and DPD1 will always read 0. The I/O direction register of PD0, PD1 and PB2 are ignored. Pull up or down resistors are still available.

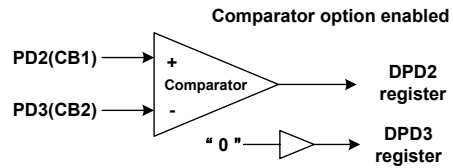
This OP Amp will be powered down in HALT mode automatically.



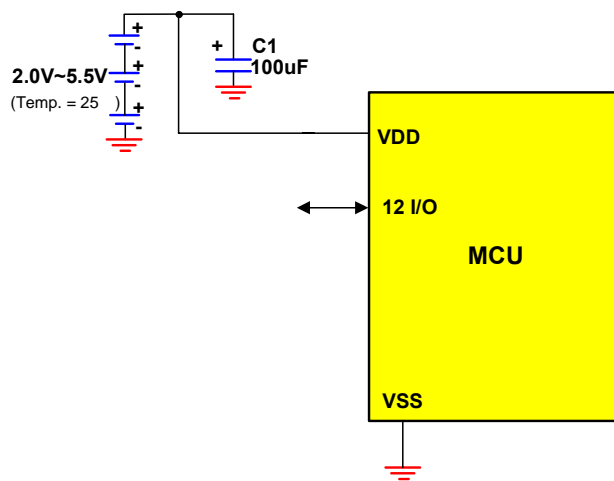


PD2, PD3 are shared with input of a Comparator

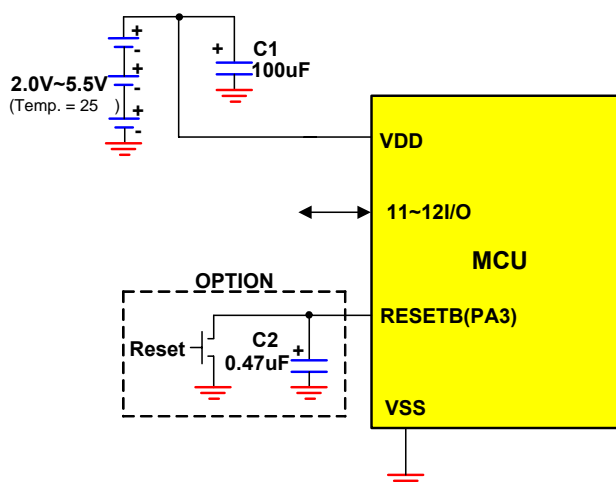
There is one comparator in TR4P153BT/BF. The input pin of comparator are shared with PD2 and PD3 pin by option. If the comparator option is enabled, the connection of external pin, internal register and comparator are as shown. The output of comparator is connected to register DPD2, and register DPD3 is always fixed to 0 in this mode. The I/O direction register of PD2 and PD3 are ignored (PD2 and PD3 will be forced as input port by hardware). Pull up or down resistors are still available. This comparator will be automatically powered down in HALT mode.



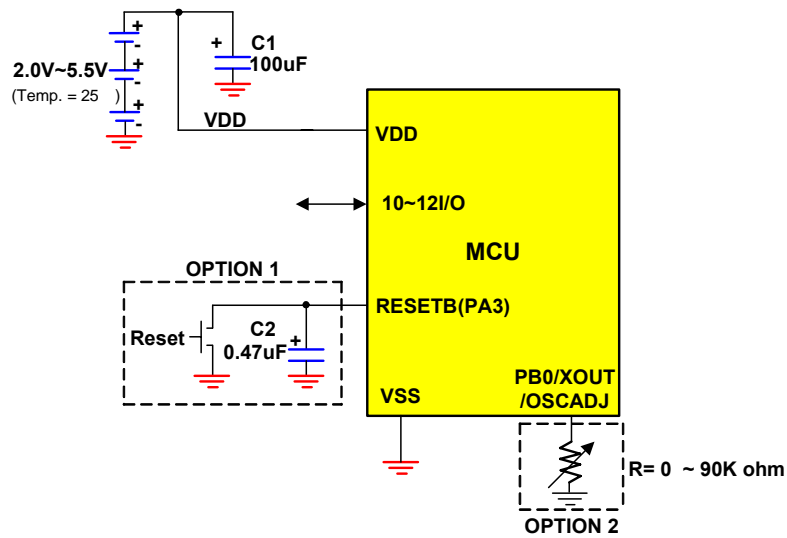
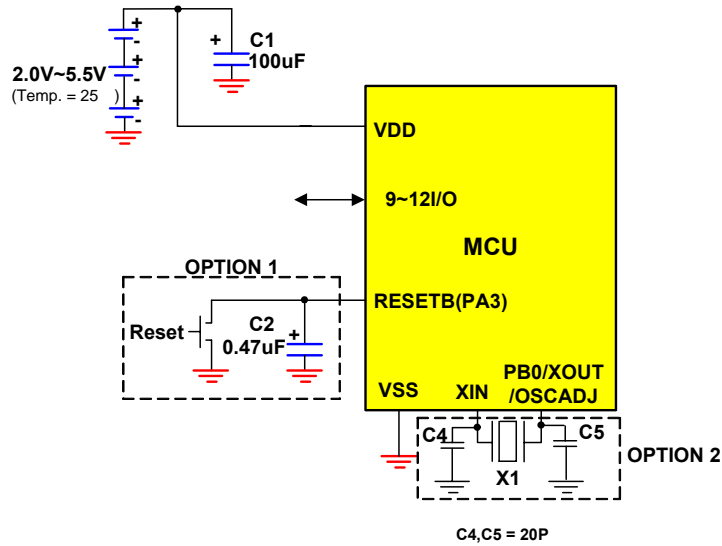
6. Application Circuit



Note : Substrate must be connected to VSS.



Note : Substrate must be connected to VSS.



Note : Substrate must be connected to VSS.



7. Option table

| Item | Option Name | Function Description | | | | | | | | | | | | | | | | | | | | |
|------|--|--|-----------------|--|--|-----------------------|----------------|------------------------------|---|----------------------|-----------------------------|----------------------|----------------|-----------------------------|---|----------------|-----------------------------|------|---|---------|---|-----------------|
| 1 | PA3_RESETB | Enable/disable RSTB (PA3 pin is shared with RSTB.) | | | | | | | | | | | | | | | | | | | | |
| 2 | WDT | WDT enable/disable | | | | | | | | | | | | | | | | | | | | |
| 3 | XTENB | External crystal mode enable/disable | | | | | | | | | | | | | | | | | | | | |
| 4 | MCKS1 | MCU operating clock definition (F_{MCK}) (external crystal frequency= F_{XTOSC}) | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ITEM</th> <th>Option XTENB=1 Use internal HRCOSC</th> <th>Option XTENB=0 Use external EXTOSC (F_{XTOSC})</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>MCU run 1 MIPS</td> <td>MCU run $F_{XTOSC} /16$ MIPS</td> </tr> <tr> <td>2</td> <td>MCU run 2 MIPS</td> <td>MCU run $F_{XTOSC} /8$ MIPS</td> </tr> <tr> <td>3</td> <td>MCU run 4 MIPS</td> <td>MCU run $F_{XTOSC} /4$ MIPS</td> </tr> <tr> <td>4</td> <td>MCU run 8 MIPS</td> <td>MCU run $F_{XTOSC} /2$ MIPS</td> </tr> </tbody> </table> | ITEM | Option XTENB=1 Use internal HRCOSC | Option XTENB=0 Use external EXTOSC (F_{XTOSC}) | 1 | MCU run 1 MIPS | MCU run $F_{XTOSC} /16$ MIPS | 2 | MCU run 2 MIPS | MCU run $F_{XTOSC} /8$ MIPS | 3 | MCU run 4 MIPS | MCU run $F_{XTOSC} /4$ MIPS | 4 | MCU run 8 MIPS | MCU run $F_{XTOSC} /2$ MIPS | | | | | |
| ITEM | Option XTENB=1 Use internal HRCOSC | Option XTENB=0 Use external EXTOSC (F_{XTOSC}) | | | | | | | | | | | | | | | | | | | | |
| 1 | MCU run 1 MIPS | MCU run $F_{XTOSC} /16$ MIPS | | | | | | | | | | | | | | | | | | | | |
| 2 | MCU run 2 MIPS | MCU run $F_{XTOSC} /8$ MIPS | | | | | | | | | | | | | | | | | | | | |
| 3 | MCU run 4 MIPS | MCU run $F_{XTOSC} /4$ MIPS | | | | | | | | | | | | | | | | | | | | |
| 4 | MCU run 8 MIPS | MCU run $F_{XTOSC} /2$ MIPS | | | | | | | | | | | | | | | | | | | | |
| 5 | MCKS0 | | | | | | | | | | | | | | | | | | | | | |
| 6 | PROTECT | OTP data lock bit enable/disable | | | | | | | | | | | | | | | | | | | | |
| 7 | IREN | Enable/disable IR 38K (PA1 is shared with IR 38K clock output.) | | | | | | | | | | | | | | | | | | | | |
| 8 | WDTHEN | WDT always enabled or not, even in HALT mode. | | | | | | | | | | | | | | | | | | | | |
| 9 | WDTS1 | WDT period definition | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ITEM</th> <th>WDT Period</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0.125 \pm12% Sec</td> </tr> <tr> <td>2</td> <td>0.25 \pm12% Sec</td> </tr> <tr> <td>3</td> <td>0.5 \pm12% Sec</td> </tr> <tr> <td>4</td> <td>1.0 \pm12% Sec</td> </tr> </tbody> </table> | ITEM | WDT Period | 1 | 0.125 \pm 12% Sec | 2 | 0.25 \pm 12% Sec | 3 | 0.5 \pm 12% Sec | 4 | 1.0 \pm 12% Sec | | | | | | | | | | |
| ITEM | WDT Period | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0.125 \pm 12% Sec | | | | | | | | | | | | | | | | | | | | | |
| 2 | 0.25 \pm 12% Sec | | | | | | | | | | | | | | | | | | | | | |
| 3 | 0.5 \pm 12% Sec | | | | | | | | | | | | | | | | | | | | | |
| 4 | 1.0 \pm 12% Sec | | | | | | | | | | | | | | | | | | | | | |
| 10 | WDTS0 | | | | | | | | | | | | | | | | | | | | | |
| 11 | LOSCS1 | MCU operating clock definition in GREEN mode | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ITEM</th> <th>MCU GREEN mode clock</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>114.69 \pm12% KIPS</td> </tr> <tr> <td>2</td> <td>57.34 \pm12% KIPS</td> </tr> <tr> <td>3</td> <td>28.67 \pm12% KIPS</td> </tr> <tr> <td>4</td> <td>14.33 \pm12% KIPS</td> </tr> </tbody> </table> | ITEM | MCU GREEN mode clock | 1 | 114.69 \pm 12% KIPS | 2 | 57.34 \pm 12% KIPS | 3 | 28.67 \pm 12% KIPS | 4 | 14.33 \pm 12% KIPS | | | | | | | | | | |
| ITEM | MCU GREEN mode clock | | | | | | | | | | | | | | | | | | | | | |
| 1 | 114.69 \pm 12% KIPS | | | | | | | | | | | | | | | | | | | | | |
| 2 | 57.34 \pm 12% KIPS | | | | | | | | | | | | | | | | | | | | | |
| 3 | 28.67 \pm 12% KIPS | | | | | | | | | | | | | | | | | | | | | |
| 4 | 14.33 \pm 12% KIPS | | | | | | | | | | | | | | | | | | | | | |
| 12 | LOSCS0 | | | | | | | | | | | | | | | | | | | | | |
| 13 | IRNOR0 | PA1 pin keep high or low when option IREN enabled and F38K register = 0(38K stopped) | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>No.</th> <th>IRNOR0 option</th> <th>F38K register</th> <th>PA1 output pin</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>disabled</td> <td>0</td> <td>low</td> </tr> <tr> <td>2</td> <td>disabled</td> <td>1</td> <td>38k square wave</td> </tr> <tr> <td>3</td> <td>enabled</td> <td>0</td> <td>high</td> </tr> <tr> <td>4</td> <td>enabled</td> <td>1</td> <td>38k square wave</td> </tr> </tbody> </table> | No. | IRNOR0 option | F38K register | PA1 output pin | 1 | disabled | 0 | low | 2 | disabled | 1 | 38k square wave | 3 | enabled | 0 | high | 4 | enabled | 1 | 38k square wave |
| No. | IRNOR0 option | F38K register | PA1 output pin | | | | | | | | | | | | | | | | | | | |
| 1 | disabled | 0 | low | | | | | | | | | | | | | | | | | | | |
| 2 | disabled | 1 | 38k square wave | | | | | | | | | | | | | | | | | | | |
| 3 | enabled | 0 | high | | | | | | | | | | | | | | | | | | | |
| 4 | enabled | 1 | 38k square wave | | | | | | | | | | | | | | | | | | | |
| 14 | RTCEN | RTC function enable/disable | | | | | | | | | | | | | | | | | | | | |
| 15 | OADJENB | PB0 is shared with OSCADJ PIN (Adj. pin of HRCOSC) or not | | | | | | | | | | | | | | | | | | | | |
| 16 | IADJENB | Enable/disable Internal frequency adjust function of HRCOSC. | | | | | | | | | | | | | | | | | | | | |
| 17 | ADJ1 | Adjust frequency range of internal HRCOSC, ADJ1 and ADJ0 is valid after IADJENB is enabled | | | | | | | | | | | | | | | | | | | | |
| 18 | ADJ0 | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>ITEM</th> <th>Internal HRCOSC frequency</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>32MHz -4%</td> </tr> <tr> <td>2</td> <td>32MHz -2%</td> </tr> <tr> <td>3</td> <td>32MHz +2%</td> </tr> <tr> <td>4</td> <td>32MHz +4%</td> </tr> </tbody> </table> | ITEM | Internal HRCOSC frequency | 1 | 32MHz -4% | 2 | 32MHz -2% | 3 | 32MHz +2% | 4 | 32MHz +4% | | | | | | | | | | |
| ITEM | Internal HRCOSC frequency | | | | | | | | | | | | | | | | | | | | | |
| 1 | 32MHz -4% | | | | | | | | | | | | | | | | | | | | | |
| 2 | 32MHz -2% | | | | | | | | | | | | | | | | | | | | | |
| 3 | 32MHz +2% | | | | | | | | | | | | | | | | | | | | | |
| 4 | 32MHz +4% | | | | | | | | | | | | | | | | | | | | | |
| 19 | OPEN | OP enable/disable | | | | | | | | | | | | | | | | | | | | |
| 20 | COMPEN | Comparator enable/disable | | | | | | | | | | | | | | | | | | | | |
| 21 | SPUP | Enable/disable : RTC time period speed up. | | | | | | | | | | | | | | | | | | | | |



8. Revision History

| Version | Description | Page | Date |
|---------|--|----------------------------------|-------------|
| 1.0 | Established | | Oct,21 2011 |
| 1.1 | 1. Delete 32K X'tal oscillator | P1,P4,P5,P14,P15 P21,P26, P27 | Dec.6 2011 |
| | 2. The three instructions mention above are two cycle instruction, others are only single cycle instruction. | P6 | |
| 1.2 | Description change | all pages | Feb.9 2012 |
| | MDCTL change to Write only | 10,13 | |
| 1.3 | 1. Operating current (VDD=3V , MCU run 114.7 KIPS) | P4 | May.8 2012 |
| | 2. AC Characteristics of OP & Comparator | P6 | |
| | 3. The LRCOSC frequency VS. temperature | P6 | |
| | 4. The HRCOSC frequency VS. temperature | P7 | |
| | 5. Modify picture --- reload | P17,P20 | |
| | 6. frequency adjust range table by OSCADJ PIN | P23 | |
| | 7.the device would not guarantee frequency deviation range | P23 | |