PT5108

High-PSRR 500mA LDO

GENERAL DESCRIPTION

The PT5108 is a low-dropout voltage regulator designed for portable applications that require both low noise performance and board space. Its PSRR at 1kHz is better than 70dB. The PT5108's performance is ideal for battery powered systems for delivering low dropout voltage and low quiescent current. An optional external bypass capacitor reduces the output noise and increases PSRR.

The device can be used for mobile phone and similar battery powered wireless applications. It provides up to 500mA, from a 2.5V to 5.5V input. The PT5108 consumes less than 0.1μA in shutdown mode and has fast turn-on time less than 150μs. The PT5108 is available in 5 pin SOT-23 package (Pd free). Selected performances are specified for −40°C to +85°C temperature range. The output voltage is available in the range of 1.5V to 5.0V.

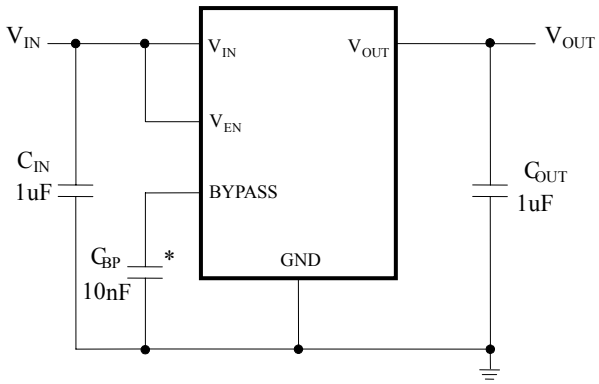
FEATURES

- 2.5V to 5.5V input range
- 72dB PSRR @1kHz, Vin = Vout + 1V
- < 1uA quiescent current at shutdown mode
- Fast turn on time: 150us (typical)
- 290mV maximum dropout voltage with 400mA load
- Thermal shutdown and short-circuit current limit
- 1.5, 1.8, 2.0, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.2V, 3.3V, 4.7V, 4.8V, 4.9V and 5.0V output standard
- Miniature SOT-23-5 package (Pd free)

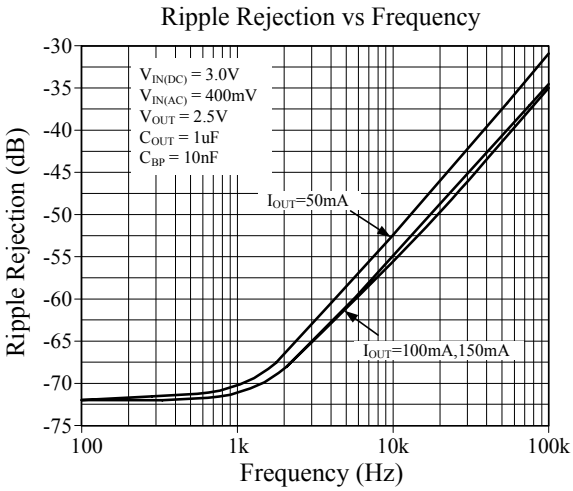
APPLICATIONS

- CDMA/GSM mobile phone
- Handless telephone
- WLAN and Bluetooth appliances
- PDAS/MP3 handsets
- Battery powered portable devices

TYPICAL APPLICATIONS



C_{OUT}: Recommended ceramic capacitor
C_{BP}: The optional bypass capacitor for noise reduction

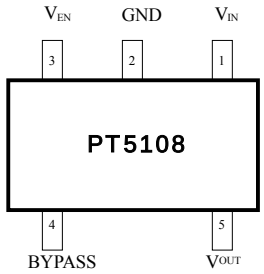


ORDERING INFORMATION*

Package	Temperature Range	Output Voltage (V)	Part Number
SOT-23-5	-40°C to 85°C	1.5	PT5108E23E-15
		1.8	PT5108E23E-18
		2.0	PT5108E23E-20
		2.5	PT5108E23E-25
		2.6	PT5108E23E-26
		2.8	PT5108E23E-28
		2.85	PT5108E23E-285
		2.9	PT5108E23E-29
		3.0	PT5108E23E-30
		3.1	PT5108E23E-31
		3.2	PT5108E23E-32
		3.3	PT5108E23E-33
		4.7	PT5108E23E-47
		4.8	PT5108E23E-48
		4.9	PT5108E23E-49
		5.0	PT5108E23E-50
		2.0	PT5108E23E-20

* All parts are supplied as 3000 units, tape and reel.

PACKAGES



SOT23-5

PIN DESCRIPTIONS

Name	SOT-23	Description
V_{IN}	1	Input of LDO
GND	2	Ground
V_{EN}	3	Enable Input Logic, Enable High
BYPASS	4	Optional bypass capacitor for noise reduction
V_{OUT}	5	Output of LDO

SIMPLIFIED BLOCK DIAGRAM

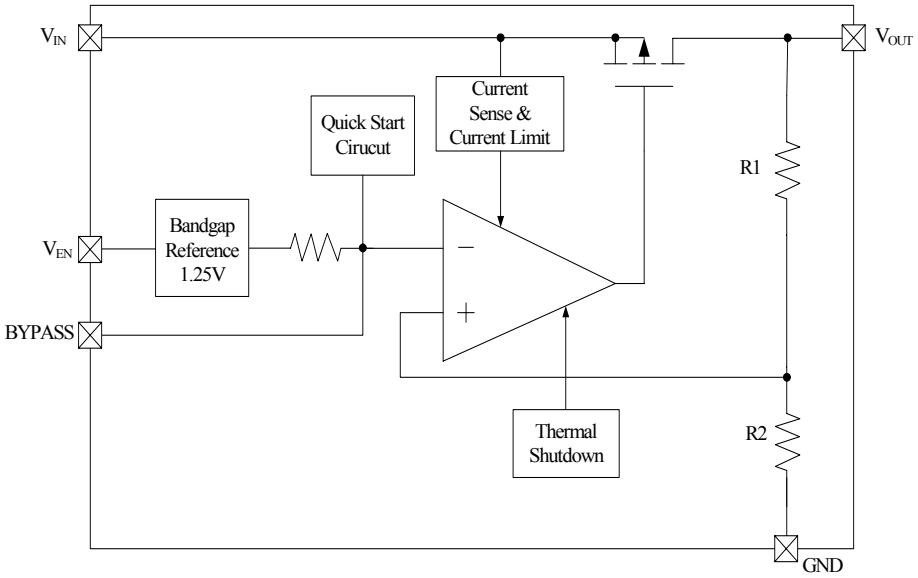


Figure 1. Graph the PT5108 major functional blocks

In Figure 1, the block of Bandgap Reference provides the reference voltage of the LDO.

The resistor and bypass capacitor connected to the BYPASS pin together form a low pass filter to attenuate the noise generated at the reference block.

The Quick Start Circuit block injects a short-time current to charge the bypass capacitor very fast during the turn-on period for the purpose of speed up the output voltage settlement. The fast charging stops when the bypass capacitor voltage reaches 95% of 1.23V (typical).

The op amp block is used as the error amplifier of the LDO by compare the reference with the output feedback voltages. Its output controls the gate of a large PMOS driver and hereby adjusts the output voltage.

The resistor R_1 and R_2 form a voltage divider to provide the feedback voltage.

The Current Sense & Limit block senses the LDO output current and limits the output current from being too high. This is mostly a short circuit protection feature.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		VALUE	UNIT
V_{IN} Range		-0.3~6.0V	V
V_{OUT} Range		-0.3~(V_{IN}+0.3)< 6.0V	V
V_{EN} Range		-0.3~6.0V	V
Maximum Power Dissipation (Note1)	SOT23-5	364	mW
Junction Temp.		150	°C
Storage Temp.		-65~150	°C
Lead Temp. (Note2)		235	°C
ESD Rating, HBM		2	KV

OPERATING RANGE

PARAMETER		VALUE	UNIT
V_{IN} Range		-0.3~5.5V	V
V_{EN} Range		-0.3~(V_{IN}+0.3)<5.5V	V
Thermal Resistance, θ_{JA}	SOT23-5	220	°C/W
Maximum Power Dissipation (Note 3)	SOT23-5	250	mW
Operation Temp.		-40~85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{IN} = $V_{OUT(nom)}$ + 0.5V, V_{EN} = V_{IN}, C_{IN} = 1 uF, I_{OUT} = 1mA, C_{OUT} = 1 uF, C_{BYPASS} = 0.01 uF， T_A = +25°C. Limits appearing in **boldface type** apply over the entire junction temperature range for operation, −40˚C to +85˚C. (Note 4) (Note5)

Symbol	Parameter	Conditions			Typ.	Min.	Max.	Unit
ΔV_{OUT}	Output Voltage Error	I_{OUT} = 1mA				-2	2	$\%V_{OUT}$
	Line Regulation Error	V_{IN}=($V_{OUT(nom)}$ + 0.5V) to 5.5V			0.02	-0.07 **-0.1**	0.07 **0.1**	%/V
	Load Regulation Error (Note 6)	I_{OUT} = 1mA to 150 mA			0.0023		0.006 **0.04**	%/mA
PSRR	Power Supply Rejection Ratio (Note 7)	V_{IN} = $V_{OUT(nom)}$ + 1.0V f = 1kHz	C_{BYPASS} = 0.01 uF	I_{OUT} = 50mA	72			dB
				I_{OUT} = 150mA	72			
			C_{BYPASS} = 0	I_{OUT} = 50mA	65			
				I_{OUT} = 150mA	65			
I_Q	Quiescent Current	I_{OUT} = 0 mA， V_{OUT} = 2.5V			90		113	uA
		I_{OUT} = 1mA to 150 mA			120		167	
		V_{EN} = 0V			0.1		1.0	
V_{DIFF}	Dropout Voltage (Note 8)	I_{OUT} = 50 mA			26		42	mV
		I_{OUT} = 100 mA			53		76 **83**	
		I_{OUT} = 150 mA			80		116 **182**	
		I_{OUT} = 400 mA			230		290	
I_{SC}	Output Short Current Limit	Output Grounded			600			mA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT}≥$V_{OUT(nom)}$ − 5%			550	300		mA
T_{ON}	Turn-On Time (Note 9)	C_{BYPASS} = 0.01 uF			150			us
	Output Noise Density	C_{BP} = 0, f = 100 kHz			200			nV/√Hz
I_{EN}	Maximum Input Current at V_{EN}	V_{EN} = 0.4 and V_{IN} = 5.5			±1			nA
V_{IL}	Maximum Low Input Level at V_{EN}	V_{IN} = 2.5 to 5.5					0.4	V
V_{IH}	Minimum High Input Level at V_{EN}	V_{IN} = 2.5 to 5.5				1.4		V
TSD	Thermal Shutdown Temperature				160			°C
	Thermal Shutdown Hysteresis				20			°C
$\Delta V_{OUT}/V_{OUT}$	V_{OUT} Temperature Characteristics	Temperature = -40 to 125°C			70			ppm/°C

Note 1: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula: $P_D = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 364mW rating for SOT23-5 appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, 150˚C, for T_J, 70˚C for T_A, and 220˚C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70˚C. Less power can be dissipated safely at ambient temperatures above 70˚C. The Absolute Maximum power dissipation can be increased by 4.5mW for each degree below 70˚C, and it must be derated by 4.5mW for each degree above 70˚C.

Note 2: Additional information on lead temperature and pad temperature may be obtained by contact CR PowTech

Note 3: Like the Absolute Maximum power dissipation, the maximum power dissipation for operation depends on the ambient temperature. The 250mW rating for SOT23-5 appearing under Operating Ratings results from substituting the maximum junction temperature for operation, 125˚C, for T_J, 70˚C for T_A, and 220˚C/W for θ_{JA} above. More power can be dissipated at ambient temperatures below 70˚C. Less power can be dissipated at ambient temperatures above 70˚C. The maximum power dissipation for operation can be increased by 4.5mW for each degree below 70˚C, and it must be derated by 4.5mW for each degree above 70˚C.

Note 4: The target output voltage, which is labeled $V_{OUT(nom)}$, is the desired voltage option.

Note 5: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with T_J = 25˚C or correlated using statistical quality control methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 6: An increase in the load current results in a slight decrease in the output voltage and vice versa.

Note 7: The PRSS is measured by applying a $50mV_{P-P}$ sine wave on V_{IN} and measure the ripple at V_{OUT} (see Figure 2).

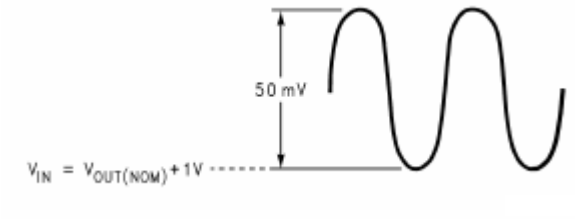


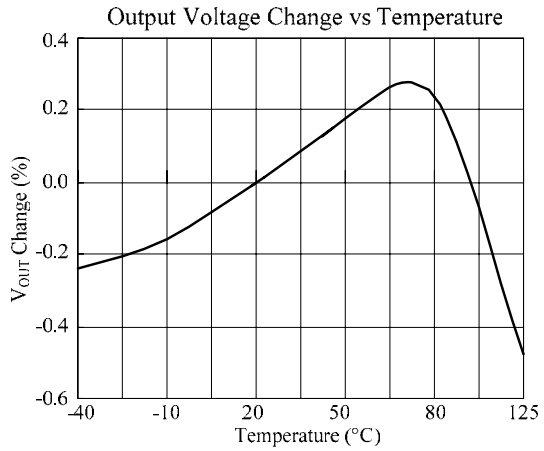
Figure 2. Graph show the sine waveform added on V_{IN} to measure PSRR

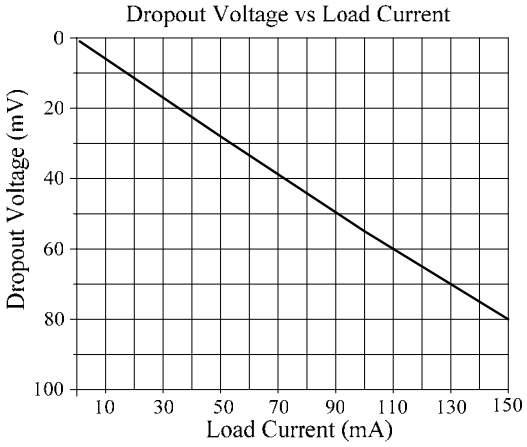
Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value. This specification does not apply for input voltages below 2.5V.

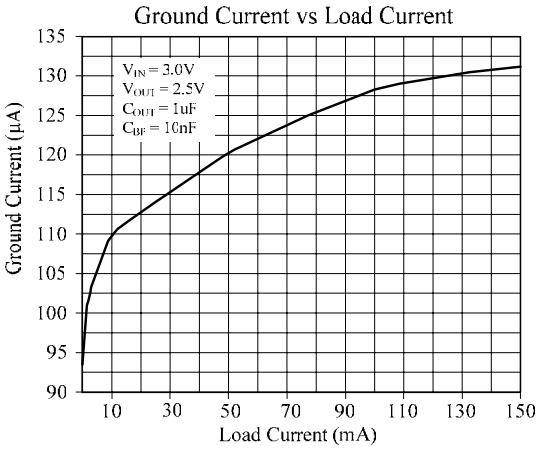
Note 9: Turn-on time is time measured between the enable input just exceeding VIH and the output voltage just reaching 95% of its nominal value.

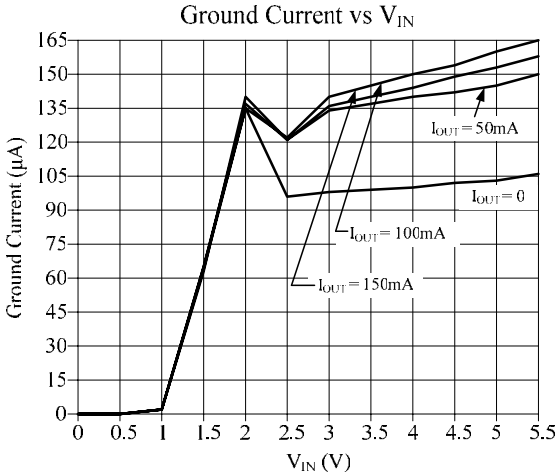
TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $V_{IN} = V_{OUT(nom)} + 0.2V$, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT} = 1$ uF Ceramic, $C_{BYPASS} = 0.01$ uF， $T_A =$ +25°C, Enable pin is tied to V_{IN}.

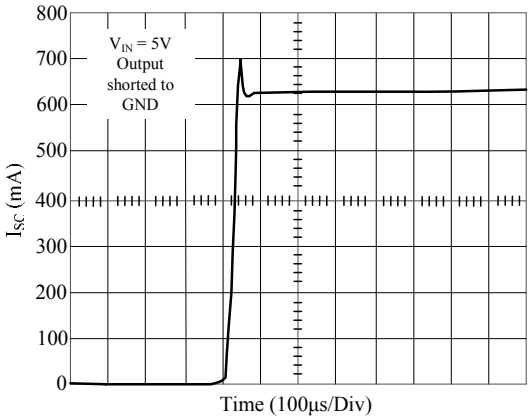




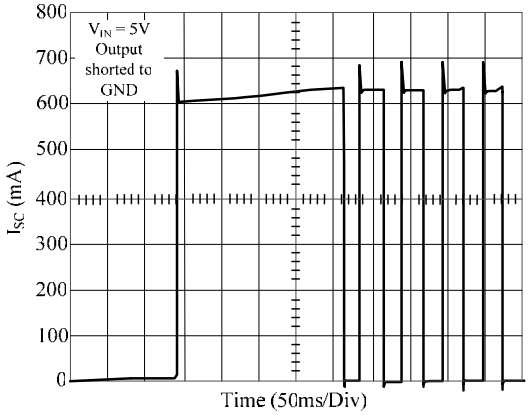




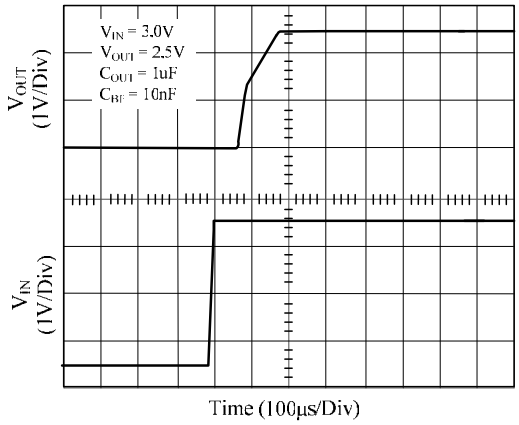
Short Circuit Current



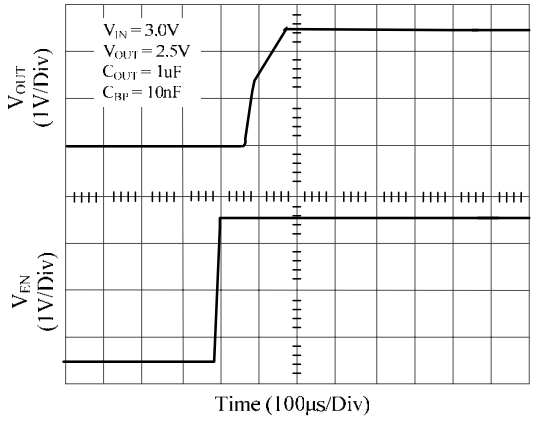
Short Circuit Current



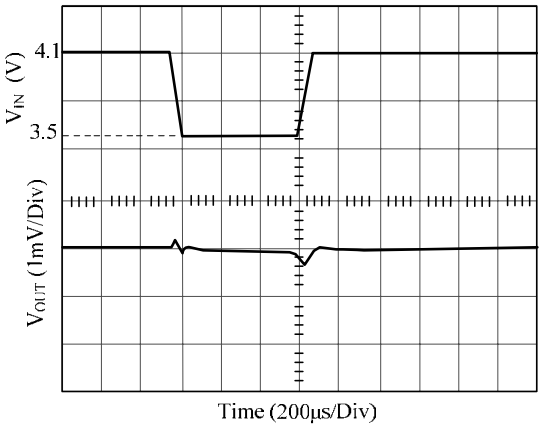
Start Up Time



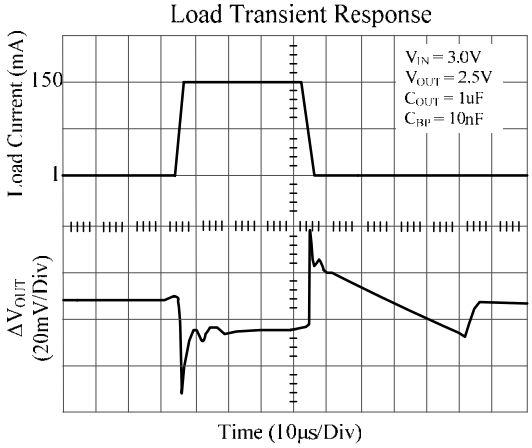
Enable Response



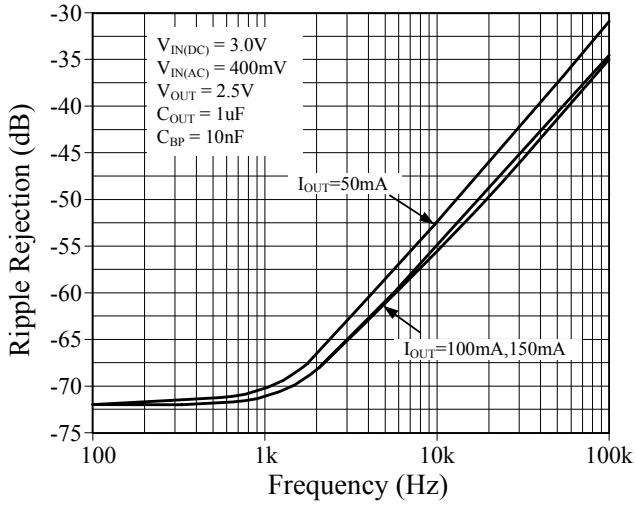
Line Transient Response



Load Transient Response



Ripple Rejection vs Frequency



APPLICATION INFORMATION

INPUT CAPACITOR

AN input capacitor of ≥ 1.0μF is required between the PT5108 V_{IN} and GND pin. This capacitor must be located within 1cm distance from V_{IN} pin and connected to a clear ground. A ceramic capacitor is recommended although a good quality tantalum or film may be used at the input. However, a tantalum capacitor can suffer catastrophic failures due to surge current when connected to a low impedance power supply (such as a battery or a very large capacitor).

There is no requirement for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered in order to ensure the capacitor work within the operation range over the full range of temperature and operating conditions.

OUTPUT CAPACITOR

In applications, it is important to select the output capacitor to keep the PT5108 in stable operation. The output capacitor must meet all the requirements specified in the following recommended capacitor table over all conditions in applications. The minimum capacitance for stability and correct operation is 0.6μF. The capacitance tolerance should be ±30% or better over the operation temperature range. The recommended capacitor type is X7R to meet the full device temperature specification.

Recommended Output Capacitor (C_{OUT})

	TYP	MIN	MAX	Unit
Capacitance	1.0	0.6	10	μF
ESR		0	400	mΩ

The capacitor application conditions also include DC-bias, frequency and temperature. Unstable operation will result if the capacitance drops below minimum specified value (see the next section Capacitor Characteristics).

The PT5108 is designed to work with very small ceramic output capacitors. A 1.0μF capacitor (X7R type) with ESR type between 0 and 400mΩ is suitable in the PT5108 applications. X5R capacitors may be used but have a narrow temperature range. With these and other capacitor types (Y5V, Z6U) that may be used, selection relies on the range of operating conditions and temperature range for a specified application.

It may also be possible to use tantalum or film capacitors at the output, but these are not as good for reasons of size and cost.

It is also recommended that the output capacitor be located within 1cm from the output pin and return to a clean ground wire.

CAPACITOR CHARACTERISTICS

The PT5108 is designed to work with ceramic capacitor on the output to take advantage of the benefit they offer: for capacitor values from 1.0μF to 4.7uF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which is good for eliminating high frequency noise). The ESR of a typical 1uF ceramic capacitor is in the range of 20mΩ to 40mΩ that easily satisfies the ESR requirement for stability by the PT5108.

For both input and output capacitors careful understanding the capacitor specifications is required to ensure correct device operation. The capacitor value can change greatly because of the operating condition and capacitor type. In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is satisfied for the application. Capacitor values can vary with DC bias conditions, temperature, and frequency of operation. Capacitor values will also demonstrate some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller size giving poorer performance figures on general.

As an example, the following figure shows a typical graph showing a comparison of capacitor case sizes in Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC bias condition the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table. It is also recommended that the capacitor manufacture's specification for the normal value capacitor are consulted for all conditions as some capacitor sizes may not be suitable in the actual application.

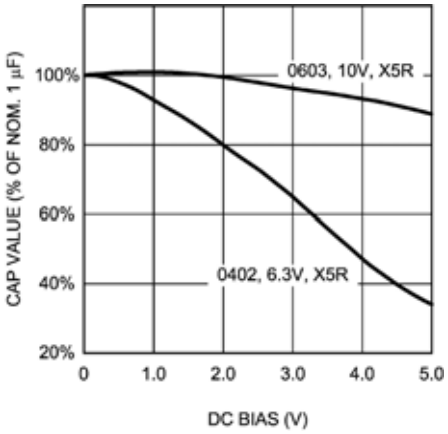


Figure 3. Graph showing a typical variation in capacitance vs. DC bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55˚C to +125˚C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55˚C to +85˚C. Most large value ceramic capacitors () 2.2µF) are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25˚C to 85˚C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25˚C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to −40˚C, so some guard band must be allowed.

NOISE BYPASS CAPACITOR

Connecting a 0.01µF capacitor between the C_{BYPASS} pin and ground significantly reduces noise on the regulator output. This capacitor is connected directly to a high impedance node in the internal reference circuit. Any significant loading on this node will cause a change on the regulated output voltage. For this reason, DC leakage current through this pin must be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. Polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current. The addition of a noise reduction capacitor does not affect the load transient response of the device.

NO-LOAD STABILITY

The PT5108 will remain stable and in regulation with no external load. This is especially important in CMOS RAM keep-alive applications.

ON/OFF INPUT OPERATION

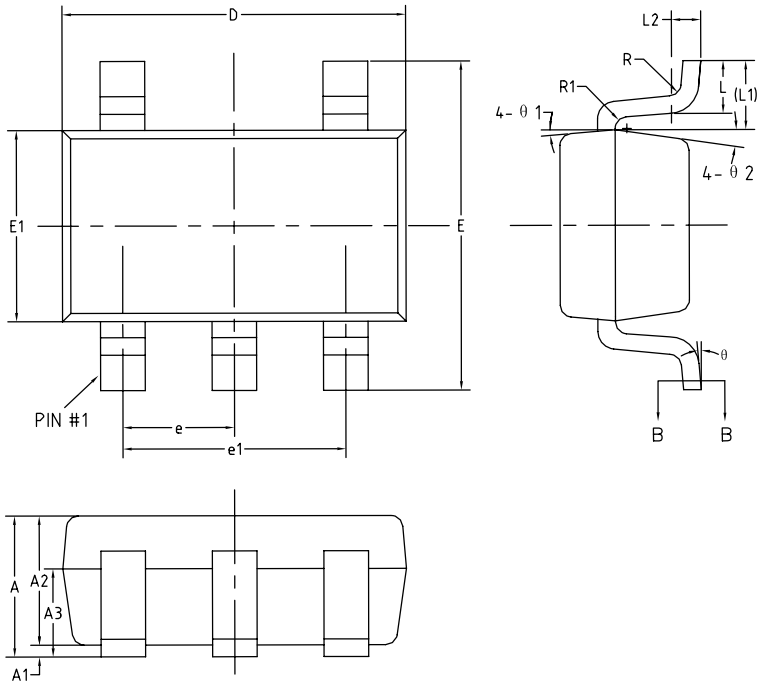
The PT5108 is turned off by pulling the V_{EN} pin low, and turned on by pulling it high. If this function is not used, the V_{EN} pin should be tied to V_{IN} to keep the regulator output on at all time. To assure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

FAST ON-TIME

The PT5108 output is turned on after V_{ref} voltage reaches its final value (1.23V typical). To speed up this process, the noise reduction capacitor at the bypass pin is charged with an internal current source. The current source is turned off when the reference voltage reaches approximately 95% of its final value. The turn on time is determined by the time constant of the bypass capacitor. The smaller the capacitor value, the shorter the turn on time, but less noise gets reduced. As a result, turn on time and noise reduction need to be taken into design consideration when choosing the value of the bypass capacitor.

PACKAGE INFORMATION

■ SOT23-5



Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.95BSC		
e1	1.90BSC		
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	3°	5°	7°
θ2	6°	8°	10°